OC65550

HiQV32™ Series
VGA BIOS

OEM Reference Guide
Revision 1.4

May 1997

P R E L I M I N A R Y

CHIPS®

Revision History

Revision	Date	By	Comment
0.1	10/6/95	RN/lc	Initial Release
0.2	12/19/95	LC	Format changes only. Removed Confidential and NDA markings. Converted to a mirrored margin page format. Renumbered pages to include chapter numbers.
1.0	3/7/96	BB/JC/lc	Official Release. Updated and added VESA Extended BGA BIOS functions. Updated and added Hooks for the System BIOS. Updated BMP frames. Updated and merged mode tables. Updated Appendix B. Added numbered sections.
1.1	4/23/96	JC/lc/bjb	Added NSTC/PAL Support function and Notify Display Switch Hook. Updated Get F65550 Information function. Added Index. Corrected errors in section numbering. Added section VESA DDC Read and Write Function Hook 5F48h Updated Extended Video Modes tables Expanded Enable Pop-Up 14h Added X, Y Pop-Up Position 14h Updated BMP tables
1.2	5/14/96	JC/bjb	Updated BMP section
1.3	9/13/96	JC/bjb	Updated BIOS Function Calls and OEM Utilities Update Extended Video Modes
1.4	5/23/97	JC/lc	Reorganized chapters, updated 5F14h, 5F50h, 4F00h, functions and 5F36h hook.

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FORWARD

This manual provides Original Equipment Manufacturers (OEMs) and end-users with information describing the functions and features of the OC65550 Super VGA BIOS .

Terminology And Conventions

`COURIER FONT`	This font is used to specify commands typed by the user, as well as output produced by the system.
Italic Type	This type style is used to denote titles. It is also used to denote computer program names, menu alternatives and other items at their first occurrence.
[]	Items enclosed in square brackets are optional and may be ignored.
<>	Items enclosed in less than and greater than symbols are keystrokes the user should type.
h	An “h” which immediately follows a number indicates the value is hexadecimal.
Bordered	Denotes important points.

About This Manual

This manual contains five chapters and three appendices. The purpose of each is as follows:

Chapter 1:	Summarizes the features of the VGA BIOS and the BIOS kits.
Chapter 2:	Describes the features of the VGA BIOS.
Chapter 3:	Explains the hardware requirements of the VGA BIOS.
Chapter 4:	Describes the standard function calls, extensions to the standard function calls and extended function calls of the VGA BIOS.
Chapter 5:	Explains the use of the OEM utility programs provided in the BIOS kits.
Appendix A:	Explains how to create a binary version of the VGA BIOS from source code.
Appendix B:	Explains how to implement the Suspend/Resume Procedure in the system BIOS.

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CHAPTER 1 - INTRODUCTION TO THE VGA BIOS

1.1. VGA BIOS

The OC65550 VGA BIOS (hereafter referred to as 65550 BIOS) is an enhanced, high performance BIOS that is used with the HiQV32™ VGA Flat Panel/CRT Controller to provide an integrated Flat panel VGA solution. The BIOS is optimized for HiQV32™ VGA Flat Panel/CRT Controller and provides:

- Full compatibility with the IBM VGA BIOS
- Support for monochrome LCD, 640x480 STN or TFT, 800x600 STN or TFT, 1024x768 TFT or STN and 1280x1024 TFT displays. Optional support for other displays.
- Supports VESA BIOS Extensions, including VBE 2.0, VBE/DDC 1.0, and VBE/PM 1.0.
- Supports either VESA local bus or PCI bus
- Extended BIOS functions which offer easy access to HiQV32™ controller features and capabilities
- Support for simultaneous display

1.2. Customization Support

The 65550 BIOS design allows the user to customize of values in the binary version of the BIOS. This capability enables an OEM to create a custom version of the BIOS without access to the source code. Customization is accomplished with the BMP550 utility included with the BIOS kits.

1.3. BIOS Kits

The 65550 BIOS is available in three kit formats. These kits and their contents are as follows:

SE65550 VGA BIOS Evaluation Kit:

- Evaluation diskette (Evaluation copy of BIOS and utility programs)
- *OC65550 VGA BIOS OEM Reference Guide*
- Release notes
- Software Incident Report (SIR) forms

SK65550 VGA BIOS Binary Kit:

- Binary diskette (Master copy of BIOS and utility programs)
- *OC65550 VGA BIOS OEM Reference Guide*
- Release notes
- Software Incident Report (SIR) forms

SC65550 VGA BIOS Source Code Kit:

- Source code diskette
- SK65550 VGA BIOS binary kit

1.4. Licensing/Ordering CHIPS' BIOS Products

CHIPS BIOS products are licensed on a per order basis. Please contact your Chips and Technologies, Inc. sales representative for ordering information.

1.5. Customer Support

CHIPS software products are supported by field application engineers located in each sales office. If you encounter a problem, or have any questions regarding a CHIPS software product, please complete a copy of the Software Incident Report (SIR) form included with your product. Forward the completed form to the local CHIPS sales office or to the following address:

Chips and Technologies, Inc.
2950 Zanker Road
San Jose, CA 95134
Attn.: Software Product Support

FAX SIR forms to:

(408) 894-2086

CHAPTER 2 - BIOS FEATURES

The 65550 BIOS is fully compatible with the IBM VGA BIOS and contains many additional features that support the HiQV32™ Flat Panel/CRT VGA controller.

2.1 VGA BIOS Compatibility Target

The 65550 BIOS can be configured to operate in a manner compatible with an IBM PS/2 motherboard VGA BIOS or IBM AT VGA adapter BIOS. The compatibility target can be configured with the BMP550 utility program.

2.1.1 PS/2 Compatibility

If *PS/2 BIOS compatibility* is selected, direct switching between color and monochrome video modes is supported when the VGA is the only adapter in the system. The 65550 BIOS supports color modes when a secondary monochrome display adapter or Hercules adapter is installed in the system. The BIOS supports monochrome modes when a secondary CGA is installed in the system. This is the default operating mode.

2.1.2 AT Compatibility

If *AT BIOS compatibility* is selected, direct switching between color and monochrome video modes is NOT supported when the VGA is the only adapter in the system. The equipment byte must be set for color before switching from a monochrome mode to a color mode and vice-versa. The 65550 BIOS supports color modes when a secondary MDA or Hercules adapter is installed in the system. In addition, the BIOS supports monochrome modes when a secondary CGA is installed in the system.

2.2 Multiple Bus Support

The 65550 BIOS supports multiple bus specifications:

- VESA Local Bus
- PCI Local Bus, Revision 2.0

2.3 Monitor Support

The 65550 BIOS supports interlaced and non-interlaced analog monitors (VGA color, VGA monochrome), but the HiQV32™ controller does not support digital monitors.

Note: Multiple frequency monitors are supported as analog monitors.

2.4 Display Boot/Display Type Configurations

The 65550 BIOS can be configured to boot on a CRT, Flat Panel, or Simultaneous display (CRT and Flat Panel are both active). The OEM may select the display boot device by changing BIOS parameters with the BMP550 utility program. The parameters which select the boot display device also select the CRT configuration. The available display boot devices are:

- CRT Boot
- Flat Panel Boot
- Simultaneous Display Boot

2.5 Video Modes

The 65550 BIOS supports all standard VGA modes as well as a wide selection of extended modes. The following tables lists the modes and vertical refresh rates that this BIOS can support.

Table 2-1: Standard Video Display Modes

Video Mode	VESA® VBE Mode	Pixel Resolution	Color Res.	Mode Type	Display Adapter	Font Size	Char. Disp.	Dot Clock (MHz)	Horiz. Freq. (KHz)	Vert Freq (Hz)	Video Memory (KB)
00h	—	320x200	16(gray)	Text	CGA	8x8	40x25	25	31.5	70	256
		320x350	16(gray)		EGA	8x14	40x25	25	31.5	70	256
		360x400	16		VGA	9x16	40x25	28	31.5	70	256
01h	—	320x200	16	Text	CGA	8x8	40x25	25	31.5	70	256
		320x350	16		EGA	8x14	40x25	25	31.5	70	256
		360x400	16		VGA	9x16	40x25	28	31.5	70	256
02h	—	640x200	16(gray)	Text	CGA	8x8	80x25	25	31.5	70	256
		640x350	16(gray)		EGA	8x14	80x25	25	31.5	70	256
		720x400	16		VGA	9x16	80x25	28	31.5	70	256
03h	—	640x200	16	Text	CGA	8x8	80x25	25	31.5	70	256
		640x350	16		EGA	8x14	80x25	25	31.5	70	256
		720x400	16		VGA	9x16	80x25	28	31.5	70	256
04h	—	320x200	4	Graph	All	8x8	40x25	25	31.5	70	256
05h	—	320x200	4(gray)	Graph	CGA	8x8	40x25	25	31.5	70	256
		320x200	4(gray)		EGA	8x8	40x25	25	31.5	70	256
		320x200	4		VGA	8x8	40x25	25	31.5	70	256
06h	—	640x200	2	Graph	All	8x8	80x25	25	31.5	70	256
07h	—	720x350	Mono	Text	MDA	9x14	80x25	28	31.5	70	256
		720x350	Mono		EGA	9x14	80x25	28	31.5	70	256
		720x400	Mono		VGA	9x16	80x25	28	31.5	70	256
08h-0Ch	—	Reserved			-		-				
0Dh	—	320x200	16	Graph	E/VGA	8x8	40x25	25	31.5	70	256
0Eh	—	640x200	16	Graph	E/VGA	8x8	80x25	25	31.5	70	256
0Fh	—	640x350	Mono	Graph	E/VGA	8x14	80x25	25	31.5	70	256
10h	—	640x350	16	Graph	E/VGA	8x14	80x25	25	31.5	70	256
11h	—	640x480	2	Graph	VGA	8x16	80x30	25	31.5	60	256
12h	—	640x480	16	Graph	VGA	8x16	80x30	25	31.5	60	256
13h	—	320x200	256	Graph	VGA	8x8	40x25	25	31.5	70	256

Table 2-2: Extended Video Modes

Video Mode	VESA® VBE Mode	Pixel Resolution	Colors	Mode Type	Mem. Org	Font Size	Char. Disp.	Dot Clock (MHz)	Horiz. Freq. (KHz)	Vert Freq (Hz)	Video Memory (KB)
20h	120	640x480	16	Graph (L)	Pack Pix	8x16	80x30	25.175	31.5	60	256
								31.5	37.5	75	256
								36	43.3	85	256
22h	122	800x600	16	Graph (L)	Pack Pix	8x16	100x37	36	35.1	56	256
								40	37.9	60	256
								49.5	46.9	75	256
								56.25	53.7	85	256
24h	124	1024x768	16	Graph (L)	Pack Pix	8x16	128x48	44.9	35.5	43(I)	384
								65	48.4	60	384
								78.75	60	75	384
								94.5	68.7	85	384
28h	128	1280x1024	16	Graph (L)	Pack Pix	8x16	160x64	78.75	47	43(I)	640
								108	64	60	640
2Ah*	—	1600x1200	16	Graph (L)	Pack Pix	8x16	200x75	—	—	—	938
30h	101h	640x480	256	Graph (L)	Pack Pix	8x16	80x30	25.175	31.5	60	300
								31.5	37.5	75	300
								36	43.3	85	300
31h	100h	640x400	256	Graph (L)	Pack Pix	8x16	80x25	25.175	31.5	70	256
32h	103h	800x600	256	Graph (L)	Pack Pix	8x16	100x37	36	35.1	56	469
								40	37.9	60	469
								49.5	46.9	75	469
								56.25	53.7	85	469
34h	105h	1024x768	256	Graph (L)	Pack Pix	8x16	128x48	44.9	35.5	43(I)	768
								65	48.4	60	768
								78.75	60	75	768
								94.5	68.7	85	768
38h	107h	1280x1024	256	Graph (L)	Pack Pix	8x16	160x64	78.75	47	43(I)	1280
								108	64	60	1280
3Ah*	—	1600x1200	256	Graph (L)	Pack Pix	8x16	200x75	—	—	—	1875
40h	110h	640x480	32K	Graph (L)	Pack Pix	8x16	80x30	25.175	31.5	60	600
								31.5	37.5	75	600
								36	43.3	85	600
41h	111h	640x480	64K	Graph (L)	Pack Pix	8x16	80x30	25.175	31.5	60	600
								31.5	37.5	75	600
								36	43.3	85	600
42h	113h	800x600	32K	Graph (L)	Pack Pix	8x16	100x37	36	35.1	56	938
								40	37.9	60	938
								49.5	46.9	75	938
								56.25	53.7	85	938

Notes: I = Interlaced L = Linear * = Modes 2Ah and 3Ah are for flat panel only.

Table 2-2: Extended Video Modes (Continued)

Video Mode	VESA® VBE Mode	Pixel Resolution	Colors	Mode Type	Mem Org	Font Size	Char. Disp.	Dot Clock (MHz)	Horiz. Freq. (KHz)	Vert Freq (Hz)	Video Memory (KB)
43h	114h	800x600	64K	Graph (L)	Pack Pix	8x16	100x37	36	35.1	56	938
								40	37.9	60	938
								49.5	46.9	75	938
								56.25	53.7	85	938
44h	116h	1024x768	32K	Graph (L)	Pack Pix	8x16	128x48	44.9	35.5	43(I)	1536
								65	48.4	60	1536
45h	117h	1024x768	64K	Graph (L)	Pack Pix	8x16	128x48	44.9	35.5	43(I)	1536
								65	48.4	60	1536
50h	112h	640x480	16M	Graph(L)	Pack Pix	8x16	80x30	25.175	31.5	60	900
								31.5	37.5	75	900
								36	43.3	85	900
52h	115h	800x600	16M	Graph(L)	Pack Pix	8x16	100x37	36	35.1	56	1407
								40	37.9	60	1407
6Ah	102h	800x600	16	Graph	Planar	8x16	100x37	36	35.1	56	256
								40	37.8	60	256
								49.5	46.9	75	256
								56.25	53.7	85	256
64h	104h	1024x768	16	Graph	Planar	8x16	128x48	44.9	35.5	43(I)	384
								65	48.4	60	384
								78.75	60	75	384
								94.5	68.7	85	384
68h	106	1280x1024	16	Graph	Planar	8x16	160x64	78.75	47	43(I)	640
								108	64	60	640
70h	101h	640x480	256	Graph	Pack Pix	8x16	80x30	25.175	31.5	60	300
								31.5	37.5	75	300
								36	43.3	85	300
71h	100h	640x400	256	Graph	Pack Pix	8x16	80x25	25.175	31.5	70	256
72h	103h	800x600	256	Graph	Pack Pix	8x16	100x37	36	35.1	56	469
								40	37.9	60	469
								49.5	46.9	75	469
								56.25	53.7	85	469
74h	105h	1024x768	256	Graph	Pack Pix	8x16	128x48	44.9	35.5	43(I)	768
								65	48.4	60	768
								78.75	60	75	768
								94.5	68.7	85	768
78h	107h	1280x1024	256	Graph	Pack Pix	8x16	160x64	78.75	47	43(I)	1280
								108	64	60	1280

Notes: I = Interlaced L = Linear

The actual availability of any particular mode, however, depends on the capabilities of the display device, the amount of memory installed, whether operation is at 3.3 volts or 5 volts, the MCLK setting, and other system parameters. For more information on mode timings and availability, please refer to the most recent revision of the 65550/554 HiQVideo™ Series Mode Support Application Note.

2.6 Flat Panel Support

The 65550 BIOS provides support for features used in conjunction with a flat panel display. The type of flat panel display can be changed with the BMP550 utility program.

2.6.1 Vertical Compensation

The 65550 BIOS supports the following vertical compensation modes for flat panel operation:

- None — Image is top justified.
- Automatic Centering — Image is automatically centered vertically.
- Tall Font/Text Compensation — Text is compensated by stretching the font in the hardware.
- Line Replication/Graphic Compensation — Line replication stretches graphics image to fill the display.

The vertical compensation can be set by using function 5F5Eh (Set Vertical Compensation). Vertical Compensation status can be read by using function 5F50h, (See Get F65550 Information, section 4.3.11).

2.6.2 Horizontal Compensation

The 65550 BIOS supports the following horizontal compensation modes for flat panel operation:

- None — Image is left justified.
- Automatic Centering — Image is automatically centered horizontally.
- Text Compression — 720 dot wide applications can be compressed to fit on 640 horizontal resolution panels by either adding the eighth and ninth pixels or deleting the ninth pixel.
- Automatic Horizontal Expansion — 640/800 dot wide images can be automatically expanded to fill 800/1024 dot wide flat panels.

The horizontal compensation can be set with function 5F5Bh.

2.6.3 Tall Font Support

The 65550 BIOS supports a special tall font in flat panel operation that provides a larger, more readable font without the distortion that can be caused by graphics compensation. The tall font replaces the standard 8x14/8x16 VGA font and can be enabled or disabled with function 5F5Eh (Enable/Disable Text Compensation).

2.6.4 Inverse Video Switching

The 65550 BIOS supports inverted and non-inverted video display. The BIOS directly initializes the video polarity on boot. The video polarity can be switched with function 5F5Ah (Set Flat Panel Video Polarity).

2.6.5 Display Switching

The 65550 BIOS provides support for switching among a flat panel, CRT, and simultaneous display at run time. Function 5F51h (Switch Display Device) performs the switching function.

2.6.6 Simultaneous Display

The 65550 BIOS can be configured to operate an analog CRT monitor and flat panel at the same time. Function 5F51h (Switch Display Device) enables and disables simultaneous display operation.

2.6.7 Extended Save and Restore

The 65550 BIOS provides functions to save and restore the state of the HiQV32™ Flat Panel/CRT VGA controller. This includes all standard and extended registers, the memory latches and the attribute flip/flop state. The functions provided are 5FA0h (Extended BIOS Save/Restore State), 5FA1h (Save Video State), and 5FA2h (Restore Video State).

2.6.8 SMI and Hot Key Support

An alternate INT 10h entry point (word pointer) is located at 8Bh in the BIOS that will bypass the STI instruction at the beginning of the usual INT 10h handler. STI instructions are not allowed during processing of a System Management Interrupt (SMI).

The 65550 BIOS and Flat Panel Windows drivers are designed to support display switching with hot keys. The following paragraphs describe how to use the video BIOS to implement hot key display switching. The system BIOS hot key function handler should call the video BIOS switch display function (INT 10h, function 5F51h) when the switch display hot key is pressed.

If the processor is an "s" series CPU, the SMI normally handles the hot key. The system BIOS must temporarily patch the INT 10h entry point prior to calling the video BIOS during the SMI. The INT 10h vector should be set to the point to offset 8Bh in the video BIOS, bypassing the STI instruction at the beginning of the usual entry point. After the INT 10h returns to the system BIOS, the system BIOS should restore the original INT 10h vector prior to returning from the hot key interrupt.

2.6.9 Hardware Pop-Up Window Interface

The HiQV32™ VGA Flat Panel/CRT Controller has the capability of overlaying a 32x32/64x64/128x128 area of screen with the off-screen data stored in different formats. The off-screen data could be an AND/XOR format cursor (Windows or OS/2), or a monochrome 2 bit per pixel format bit map. The 65550 BIOS provides the pop-up support under SMI through the 5F14H function.

2.7 PCI Support

2.7.1 Video BIOS

The 65550 BIOS is developed for use with PCI Local Bus board configurations as defined in the *PCI Local Bus Specification, Rev 2.0.* The 65550 BIOS has word pointers to the PCI Data Structure at offset C000:18h/E000:18h. The PCI Data Structure is defined as follows:

Table 2-3 PCI Data Structure

Offset	Length	Data	Description
0	4	PCIR	Signature
4	2	102Ch	Vendor ID
6	2	00E0h	Device ID
8	2	0000h	Pointer to vital product data
A	2	0018h	PCI data structure length
C	1	00h	PCI structure rev
D	3	00h,00h,03h	Class code
10	2	0040h/50h/058h	Image Length 32K/40K/44K
12	2	0000h	Rev level of code/data
14	1	00h	Code Type
15	1	08h	Indicator
16	2	0000h	Reserved

2.7.2 System BIOS

The 65550 Flat Panel/CRT controller supports expansion ROM Base Address at offset 30h in the configuration space. The video BIOS is usually merged with the system BIOS and is located at address E000:0 in the system. To find the video device during power up, the system BIOS reads class code at offset 09h (00h,00h,3h) in the configuration space. The system BIOS then looks for PCIR signatures in the C000/E000 segment (word pointer to the PCIR string is at C000:18h/E000:18h) followed by the video device class code (00h,00h,03h) at offset 0Dh in the PCI data structure of the video BIOS. When the system BIOS finds the video device, it should map the video BIOS at a very high address, then copy the video BIOS at Address C000:0/E000:0.

Note: The 65550 BIOS should be BMPed for the correct segment.

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CHAPTER 3 - HARDWARE REQUIREMENTS

This chapter describes the external hardware requirements for the 65550 BIOS. For more information regarding hardware implementation, please refer to the *65550 High Performance Flat Panel/CRT VGA Controllers Data Sheet*, Chips and Technologies, Inc.

3.1 HiQV32™ VGA Flat Panel/CRT Controller

The 65550 BIOS requires a Chips and Technologies, Inc. HiQV32™ VGA Flat Panel/CRT Controller.

3.2 Color Palette RAMDAC

The 65550 BIOS assumes that the HiQV32™ on-chip color palette/DAC is used.

3.3 Monitor Detection Circuitry

The monitor detection circuitry should be implemented in a manner compatible with the IBM AT VGA adapter. The 65550 BIOS assumes that the monitor detection circuitry, if present, is attached to the SENSE pin of the HiQV32™ Flat Panel/CRT VGA controller.

3.4 Pixel Clocks

The 65550 BIOS requires specific clock frequencies to operate. The 65550 BIOS assumes that the on-chip clock synthesizer generates the clock signals.

Table 3-1 specifies the values for the Clock Select and Feature Control outputs necessary to use the specified clock source and the frequencies expected by the 65550 BIOS.

Table 3-1: Pixel Clock Selection Values and Frequencies

MSR or FR03 Bits 3,2	Pixel Clock Selection	Pixel Clock Frequency	Comments
0, 0	CLK0	25.175 MHz.	Program XRC0-C3
0, 1	CLK1	28.322 MHz.	Program XRC4-C7
1, X	CLK2	Variable	Program XRC8-CB

CRT Mode:

MSR = Miscellaneous Output Register (Write at 3C2h, Read at 3CCh)

Flat Panel/Simultaneous Mode:

FR03 = Extended Register (Read/Write at 3D0h-3D1h)

3.5 Memory Clock and Dot Clock

The 65550 BIOS allows the user to program the Dot Clock (Pixel Clock) and the Memory Clock using the on-chip clock synthesizer. The memory clock is programmed by using XRCC-CE.

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CHAPTER 4 - BIOS FUNCTION CALLS

4.1 Standard VGA BIOS Functions

The 65550 BIOS uses the same function and sub-function calls that are implemented in the IBM VGA BIOS.

4.2 Standard VGA BIOS Function Extensions

The 65550 BIOS provides a set of extended functions that are implemented as extensions to the standard Set Video Mode (00h), Get Video State (0Fh) (see Table 4-1), and Save/Restore Video State (1Ch) functions. They are fully supported by the other standard VGA BIOS function calls.

00h Set Video Mode

The Set Video Mode function sets the display mode used by the HiQV32™ Flat Panel/CRT VGA controller.

Calling Registers:

AH - 00h Set Video Mode

AL - Display Mode

Return Registers:

Nothing

0Fh Get Video State

The Get Video State function returns the screen width in character columns, video display mode, and active display page.

Calling Registers:

AH - 0Fh Get Video State

Return Registers:

AH - Number of Character Columns

AL - Display Mode

BH - Active Display Page

1Ch Save/Restore Video State

This function and its sub-functions save and restore specified video environment parameters (BIOS data area, color palette, and registers). The 65550 BIOS also allows the extended registers and emulation mode registers to be saved. This is specified by CX:Bit 15.

1C00h Get Save/Restore Buffer Size

Calling Registers:

AX - 1C00h Get Save/Restore Buffer Size

CX - Save/Restore Options:
- Bit 0 Video Hardware State
- Bit 1 Video BIOS Data Areas
- Bit 2 Video DAC State and Color Registers
- Bit 13 BitBLT Registers
- Bit 15 Extended Registers

Return Registers:

AL - 1Ch Function was successful

BX - Buffer Size Required in 64 byte blocks

1C01h Save Video State

Calling Registers:

AX - 1C01h Save Video State

CX - Save/Restore Options:
- Bit 0 Video Hardware State
- Bit 1 Video BIOS Data Areas
- Bit 2 Video DAC State and Color Registers
- Bit 13 BitBLT Registers
- Bit 15 Extended Registers

ES - Segment of Save Area

BX - Offset of Save Area

Return Registers:

AL - 1Ch Function was successful

1C02h Restore Video State

Calling Registers:

AX	-	1C02h Save Video State
CX	-	Save/Restore Options: Bit 0 Video Hardware State Bit 1 Video BIOS Data Areas Bit 2 Video DAC state and Color Registers Bit 13 BitBLT Registers Bit 15 Extended Registers
ES	-	Segment of Restore Area
BX	-	Offset of Restore Area

Return Registers:

AL	-	1Ch Function was successful

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CHAPTER 5 - EXTENDED BIOS FUNCTION CALLS

5.1 Extended BIOS Functions

The 65550 BIOS provides a set of function calls to control operation of the extended features of the HiQV32™ Flat Panel/CRT VGA Controller. These function calls are implemented as sub-functions under the extended VGA control function (5Fh).

Table 5-1. 65550 BIOS Extended Functions

AX	Function
5F00h	Get Controller Information
5F02h	Set Clock
5F04h	Get Refresh Rate Information
5F05h	Set Refresh Rate Information
5F10h	Get Linear Display Memory Information
5F11h	Get Memory Map I/O Information (PCI)
5F13h	Set Up Video Memory for Save/Restore
5F14h-00h	Set Pop-Up Memory Mode
5F14h-01h	Reset Pop-Up Memory Mode
5F14h-02h	Enable Pop-Up
5F14h-03h	Disable Pop-Up
5F14h-04h	Get Pop-up Memory Offset
5F14h-05h	Set X, Y Pop-Up Position
5F15h-00h	Notify Video BIOS of 3.3V/5V mixed
5F15h-01h	Notify Video BIOS of 5V mode switch
5F19h-00h	Get NTSC / PAL Support
5F19h-01h	Set NTSC / PAL Support
5F22h	Get Mode Support Information
5F50h	Get F65550 Information
5F51h	Switch Display Device
5F54h	Set Panel ON/OFF
5F55h	Monitor Detect
5F56h	Get Panel Type
5F5Ah	Set Flat Panel Video Polarity
5F5Bh	Set Horizontal Compensation
5F5Eh	Set Vertical Compensation
5FA0h	Get Save/Restore Buffer Size
5FA1h	Save Video State
5FA2h	Restore Video State

5F00h Get Controller Information

This function returns configuration information about the 65550 VGA system.

Calling Registers:

AX - 5F00h Get controller information

Return Registers:

BH - Video memory available
- 00h 0.5 MB
- 01h 1.0 MB
- 02h 1.5 MB
- 03h 2.0 MB
- 04h 2.5 MB
- 05h 3.0 MB
- 06h 3.5 MB
- 07h 4.0 MB

BL - Chip type:
2Ch (F6555X)

CX - Device ID:
00E0h (F65550)

DX - Video BIOS internal version number

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5F02h Set Clock

This function is used to program the internal clock synthesizer with a given frequency.

Calling Registers:

AX - 5F02h Set Dot Clock/Memory Clock

BH - Clock to set:
- 00h Set Dot Clock 0
- 01h Set Dot Clock 1
- 02h Set Dot Clock 2
- 03h Set Memory Clock
- FFh Program Default Dot Clock 2 and Memory Clock

BL - Clock Value:
6 to 150 MHz (decimal)

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5F04h Get Refresh Rate Information

This function returns the vertical refresh rate setting and the available vertical refresh rates for the given mode. Therefore this function does not apply to standard VGA modes 00h-13h or to NTSC/PAL modes.

Calling Registers:

AX - 5F04h Get refresh rate

BL - Mode Number

Return Registers:

BL - Available refresh rates, indicated by one or more bits set as follows:
Bit 0 Interlaced
Bit 1 56Hz
Bit 2 60Hz
Bit 3 70Hz
Bit 4 72Hz
Bit 5 75Hz
Bit 6 85Hz
Bit 7 Reserved

BH - Current refresh rate (see BL)

CX - Reserved

AX - Return Status:
Function not supported if AL != 5Fh
005Fh Function supported but failed
015Fh Function supported and successful

5F05h Set Refresh Rate Information

This function sets a new vertical refresh rate for the given mode. If the mode is currently active, the BIOS will program the CRT controller for the new refresh rate. If the mode is not active, the new refresh rate will be programmed the next time this mode is set. The refresh rates are effective in the CRT display modes only. Therefore this function does not apply to standard VGA modes 00h-13h or to NTSC/PAL modes.

Calling Register:

AX - 5F05h Set Refresh Rate

BL - Mode Number

BH - Set refresh rate, indicated by setting one bit as follows:
Bit 0 Interlaced
Bit 1 56Hz
Bit 2 60Hz
Bit 3 70Hz
Bit 4 72Hz
Bit 5 75Hz
Bit 6 85Hz
Bit 7 Reserved

CX - Reserved

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh
005Fh Function supported but failed
015Fh Function supported and successful

5F10h Get Linear Display Memory Information

This function returns information regarding the linear memory starting address, size and width.

Calling Register:

AX	-	5F10h Get Linear Display Memory Information

Return Registers:

BX	-	Display Memory Base Address (High)
CX	-	Display Memory Base Address (Low)
SI	-	Display Memory Size (High)
DI	-	Display Memory Size (Low)
DX	-	Display Width in bytes
AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F11h Get Memory Map I/O Information

This function returns information regarding memory mapped I/O on a PCI configuration.

Calling Registers:

AX	-	5F11h Get Memory Mapped I/O Information

Return Registers:

BX	-	Memory Mapped I/O Base Address (High)
CX	-	Memory Mapped I/O Base Address (Low)
SI	-	Reserved
DI	-	Reserved
DX	-	Reserved
AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F13h Set Up Video Memory For Save/Restore

This function sets up for saving/restoring all of the video memory in 64KB blocks (the appropriate 64KB block is made available at location A000:0000 for reading/writing).

Calling Registers:

AX	-	5F13h Set up Video Memory for Save/Restore
BX	-	0000h
CX	-	n-th 64K block to save/restore where (n = 0,1,2,....)

Return Registers:

AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F14h Set/Reset Pop-Up Memory Mode

The following sub-functions set or reset the pop-up memory mode.

5F14h - 00h Set Pop-Up Memory Mode

This sub-function sets the pop-up memory mode. The video BIOS saves the necessary registers in the 32-byte buffer passed by the SMI, and then sets up registers for dumping the pop-up bit map into the off-screen video memory. If the BLTer is in System to Screen BLT mode, the video BIOS may return with an error to indicate that video memory cannot be accessed at this time, and that the SMI handler should exit SMI mode in this situation.

Note: If the function is successful, then the SMI must call the Video BIOS with AX = 5F14h, BL = 01h to restore video controller registers after the SMI loads the pop-up screen into the video memory. BIOS supports up to 8 pop-up screens. The total number of pop-up support can be set by using BMP options.

Calling Registers:

AX	-	5F14h Set Pop-Up Function
BL	-	00h Set Pop-Up Memory Mode
ES:DX	-	Pointer to 32 byte buffer for Video BIOS in SMI

Return Registers:

ES:DI	-	Pointer to the first pop-up screen memory @ A000H
BL	-	00h Function Error (System to Screen BLT mode) 01h Function O.K.
BH	-	0-07h Total number of pop-up screens supported (1,2,3...8)
CX		Size of each pop-up screen in bytes
AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F14h - 01h Reset Pop-Up Memory Mode

This sub-function resets the pop-up memory mode. The Video BIOS restores all the registers changed by the *Set Pop-Up Memory Function* from the buffer passed by the SMI.

Calling Registers:

AX	-	5F14h Set Pop-Up Function
BL	-	01h Set Pop-Up Memory Mode
ES:DX	-	Pointer to 32 byte buffer for Video BIOS in SMI

Return Registers:

AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F14h - 02h Enable Pop-Up

This sub-function sets and enables the pop-up menu, and notifies the driver to use the software cursor.

Calling Registers:

AX - 5F14h Set Pop-Up Function

BL - 02h Enable Pop-Up

ES:EX - RGB Pointer to 32 byte buffer for Video BIOS in SMI Bytes

0-2	Cursor Color 0
3-5	Cursor Color 1
6-8	Cursor Color 2
9-B	Cursor Color 3
C-31	Video BIOS data area in SMI

CX - Bits

2-0	Enable Pop-Up Number		
000	1		
001	2		
010	3		
011	4		
100	5		
101	6		
110	7		
111	8		
7-3	Reserved		
8	Reserved		
11-9	Pop-Up Type		
000	Pop-Up Disabled (default)		
001	32x32	2bpp	AND/XOR
010	128x128	1bpp	2-color
011	128x128	1bpp	1-color + transparency
100	64x64	2bpp	3-color + transparency
101	64x64	2bpp	AND/XOR
110	64x64	2bpp	4-color
111	Reserved		
13-12	Cursor Position		
00	Upper Left corner		
01	Bottom Left corner		
11	Bottom Right corner		
14-15	Reserved		

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh

005Fh	Function supported but failed
015Fh	Function supported and successful

5F14h - 03h Disable Pop-Up

This sub-function disables the pop-up menu and notifies the driver to use the hardware cursor.

Calling Registers:

AX	-	5F14h Set Pop-Up Function
BL	-	03h Disable Pop-Up
ES:DX	-	Pointer to 32 byte buffer for Video BIOS in SMI

Return Registers:

AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F14h - 04h Get Pop-Up Memory Offset

This sub-function returns pop-up memory offset. This offset should be added to the video memory start address to get the absolute pop-up memory address.

Calling Registers:

AX	-	5F14h Set pop-up function
BL	-	04h Get pop-up memory offset

Return Registers:

BX	-	Pop-up memory address offset (High)
DI	-	Pop-up memory address offset (Low)
CX	-	Size of each pop-up screen in bytes
DL	-	Number of pop-ups supported minus one (00h-07h)
AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F14h - 05h Set X, Y Pop-Up Position

This sub-function specifies the pop-up position on the screen.

Calling Registers:

AX	-	5F14h	Set pop-up function
BL	-	05h	Set X, Y Position

Return Registers:

CX	-	X Position
DX	-	Y Position
AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F15h Notify Video BIOS of Voltage Mode

The following sub-functions will notify the video BIOS of the voltage mode to use.

5F15h - 00h Notify Video BIOS for 3.3V/5V Mixed Mode Switch

This sub-function notifies the Video BIOS to switch to 3.3V/5V mixed mode. If the Video BIOS cannot switch immediately, then it will set an internal flag to perform the switch later, when switching is possible.

Calling Registers:

AX	-	5F15h	Notify Video BIOS of voltage mode
BH	-	00h	3.3V/5V Mixed Mode Switch
BL	-	55h	

Return Registers:

BL - Voltage Switch Status:
- 00h Function supported, but cannot change to 3.3V at this time
- 01h Function supported, switched to 3.3V
- 55h Function not supported

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5F15h - 01h Notify Video BIOS for 5V Mode Switch

This sub-function notifies the Video BIOS to switch to 5V mode. If the Video BIOS cannot switch immediately, then it will set an internal flag to perform the switch later, when switching is possible.

Calling Registers:

AX	-	5F15h	Notify Video BIOS of voltage mode
BH	-	01h	5V Mode Switch
BL	-	55h	

Return Registers:

BL - Voltage Switch Status:
- 01h Function Supported, switched to 5V
- 55h Function not Supported

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5F19h NTSC / PAL Support

This function will set or get NTSC (National Television System Committee) or PAL (Phase Alternation Line) support. NTSC and PAL are television standards that will allow the video chipset output to be displayed on a television or other display that supports these standards. For NTSC or PAL modes to be active, the system must be set to CRT display and set in a NTSC / PAL supported mode (03h, 12h, 13h, and all extended modes).

5F19h Get NTSC / PAL Support

The Get sub-function will get the state of the NTSC / PAL flags and the current NTSC / PAL display mode. The NTSC / PAL flags (BH) show the mode that will be set when possible. These flags allow the video BIOS to appropriately activate or deactivate a NTSC or PAL mode without external intervention. The current NTSC / PAL mode (BL) shows which, if any, NTSC or PAL mode is active.

Calling Registers:

AX	-	5F19h	NTSC PAL Support
BL	-	00h	Get NTSC / PAL Support

Return Registers:

BH	-	NTSC / PAL Flag State:	
		00h	Flags set for no NTSC or PAL (normal display)
		01h	Flags set for NTSC
		02h	Flags set for PAL
BL	-	Current NTSC / PAL Mode:	
		00h	NTSC and PAL inactive
		01h	NTSC active
		02h	PAL active
AX	-	Return Status:	
		Function not supported if AL != 5Fh	
		005Fh	Function supported but failed
		015Fh	Function supported and successful

5F19h Set NTSC / PAL Support

The Set sub-function will set flags to indicate if NTSC, PAL or neither mode should be activated when an appropriate system state is entered. For this reason, this function will return a successful status even if a NTSC or PAL mode is not activated. If the system state at the time of calling this sub-function is an acceptable NTSC or PAL state, the set function will activate NTSC or PAL according to the flags. If the flags are set to disable NTSC and PAL modes, NTSC and PAL modes will be deactivated before the return of this sub-function.

Calling Registers:

AX	-	5F19h	NTSC PAL Support
BL	-	01h	Set NTSC / PAL Support
BH	-	NTSC / PAL Flags and Mode:	
		00h	Disable NTSC and PAL (normal display)
		01h	Enable NTSC
		02h	Enable PAL

Return Registers:

AX	-	Return Status:	
		Function not supported if AL != 5Fh	
		005Fh	Function supported but failed
		015Fh	Function supported and successful

5F22h Get Mode Support Information

This function returns display types that are supported by the given or current mode. It also returns the current display type. These two pieces of information can be used to determine if a mode is supported on the current display type.

Calling Registers:

AX - 5F22h Get Mode Support Information

BH - Mode to Use:
- 00h Current Mode
- 01h Mode specified in BL

BL - Mode Number

Return Registers:

BH - Current Display Mode
- Bit 0 CRT display type
- Bit 1 Flat panel display type
- Bit 2 Simultaneous display type

BL - Mode Support Information
- Bit 0 Mode supported in CRT display type
- Bit 1 Mode supported in flat panel display type
- Bit 2 Mode supported in simultaneous display type

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

CX - Mode Horizontal (x) Resolution

DX - Mode Vertical (y) Resolution

5F50h Get Panel Information

This function returns the current CRT/flat panel information.

Calling Registers:

AX - 5F50h Get Panel Information

Return Registers:

BX - Flat Panel Horizontal size in pixels

CX - Flat Panel Vertical size in pixels

DX - F65550 status:

Bit 0 Panel Type:
0 = TFT
1 = STN

Bit 1 0 = CRT
1 = Flat Panel

Bit 2 0 = Normal Video Polarity
1 = Inverted Video Polarity

Bit 3 0 = CRT/Flat Panel
1 = Simultaneous

Bit 4 = Drivers check for CRT Panning
0 = Disabled
1 = Enabled

Bits 5-7 Reserved

Bit 8 0 = Vertical Text Compensation Disabled
1 = Vertical Text Compensation Enabled

Bit 9 0 = Vertical Centering Disabled
1 = Vertical Centering Enabled

Bit 10 0 = Vertical Graphics Compensation Disabled
1 = Vertical Graphics Compensation Enabled

Bit 11 = Support NTSC / PAL functionality in applications
0 = Disabled
1 = Enabled

Bit 12 0 = VL
1 = PCI

Bit 13 0 = Horizontal Text Compensation Disabled
1 = Horizontal Text Compensation Enabled

Bit 14 0 = Horizontal Centering Disabled
1 = Horizontal Centering Enabled

Bit 15 0 = Horizontal Graphics Compensation Disabled
1 = Horizontal Graphics Compensation Enabled

Return Registers:

DI -

Bit 0 0 = Vertical Text Compensation in 350 Line Disabled
1 = Vertical Text Compensation in 350 Line Enabled
Bit 1 0 = Vertical Text Compensation in 400 Line Disabled
1 = Vertical Text Compensation in 400 Line Enabled
Bit 2 0 = Vertical Graphics Compensation in 350 Line Disabled
1 = Vertical Graphics Compensation in 350 Line Enabled
Bit 3 0 = Vertical Graphics Compensation in 400 Line Disabled
1 = Vertical Graphics Compensation in 400 Line Enabled
Bit 4 0 = Vertical Graphics Compensation in 480 Line Disabled
1 = Vertical Graphics Compensation in 480 Line Enabled
Bit 5 0 = Vertical Graphics Compensation in 600 Line Disabled
1 = Vertical Graphics Compensation in 600 Line Enabled
Bits 6-7 Reserved
Bits 8-9 Horizontal Font Expansion in Text Mode
00 8-dot to 8-dot, 9 dot to 8 dot
01 8-dot to 8-dot, 9 dot to 9 dot
10 8- or 9- dot to 9-dot if panel size is wide enough
11 8- or 9- dot to 10-dot if panel size is wide enough
Bits 10-11Reserved
Bit 12 0 = Horizontal Expansion in 640 Resolution is Disabled
1 = Horizontal Expansion in 640 Resolution is Enabled
Bit 13 0 = Horizontal Expansion in 800 Resolution is Disabled
1 = Horizontal Expansion in 800 Resolution is Enabled
Bit 14 0 = Horizontal Expansion in 1024 Resolution is Disabled
1 = Horizontal Expansion in 1024 Resolution is Enabled
Bit 15 Reserved

AX - Return Status:
Function not supported if AL != 5Fh
005Fh Function supported but failed
015Fh Function supported and successful

5F51h Switch Display Device

This function switches between CRT, flat panel, and simultaneous displays. The current panel type can be retrieved from function 5F22h.

Calling Registers:

AX	-	5F51h	Switch Display Device
BL	-	00	Switch to CRT
		01	Switch to Flat Panel
		02	Switch to Simultaneous
		03	If CRT attached toggle to next display state: LCD → CRT → Simultaneous → LCD

Return Registers:

AX	-	Return Status: Function not supported if AL != 5Fh
		005Fh Function supported but failed
		015Fh Function supported and successful

5F54h Set Panel ON/OFF

This function sets the panel ON or OFF. Power consumption is reduced in Panel OFF Mode.

Calling Registers:

AX - 5F54h Set Panel ON/OFF

BL - Power Down Mode:
00h Panel ON
01h Panel OFF

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh
005Fh Function supported but failed
015Fh Function supported and successful

5F55h Monitor Detect

This function detects the monitor type and returns the status to the caller.

Calling Registers:

AX - 5F55h Monitor Detect

BX - 0001h

Return Registers:

BL - Monitor Type:
- 00h Color CRT detected
- 01h Monochrome CRT detected
- 02h No CRT detected

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5F56h Get Panel Type

This function is used to return panel type information.

Calling Registers:

AX	-	5F56h Get Panel Type
BX	-	0000h

Return Registers:

BL	-	0, 1, 2,...7 (Panel #1, 2, 3, ...8)
AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

5F5Ah Set Flat Panel Video Polarity

This function sets the polarity of the video output to the flat-panel.

Calling Registers:

AX - 5F5Ah Set flat panel video stream polarity

BL - Flat Panel Video Polarity:
00h Normal polarity
01h Inverted polarity
02h Toggle polarity

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh
005Fh Function supported but failed
015Fh Function supported and successful

5F5Bh Set Horizontal Compensation

This function enables or disables Horizontal Graphics Expansion, Text Font Expansion and Centering.

AX - 5F5Bh Enable/Disable Horizontal Compensation

BL - Horizontal Compensation:

00h	Enable Horizontal Text Compensation
01h	Disable Horizontal Text Compensation
02h	Enable Horizontal Centering
03h	Disable Horizontal Centering
04h	Enable Horizontal Graphics Compensation
05h	Disable Horizontal Graphics Compensation
06h	Set 8-dot to 8-dot and 9-dot to 8-dot
07h	Set 8-dot to 9-dot and 9-dot to 9-dot
08h	Set 8-dot to 10-dot and 9-dot to 10-dot
09h	Enable Horizontal Graphics Compensation In 640 Col Mode
0Ah	Disable Horizontal Graphics Compensation In 640 Col Mode
0Bh	Enable Horizontal Graphics Compensation In 800 Col Mode
0Ch	Disable Horizontal Graphics Compensation In 800 Col Mode
0Dh	Enable Horizontal Graphics Compensation In 1024 Col Mode
0Eh	Disable Horizontal Graphics Compensation In 1024 Col Mode

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh

005Fh	Function supported but failed
015Fh	Function supported and successful

5F5Eh Set Vertical Compensation

This function enables or disables vertical text stretching and centering, and line replication. Use function 5F50 to get compensation status.

Calling Registers:

AX - 5F5Eh Enable/Disable Vertical Compensation

BL - Vertical Compensation:

00h	Enable Vertical Text Compensation
01h	Disable Vertical Text Compensation
02h	Enable Vertical Centering
03h	Disable Vertical Centering
04h	Enable Vertical Graphics Compensation
05h	Disable Vertical Graphics Compensation
06h	Enable Vertical Text Compensation in 350 Line
07h	Disable Vertical Text Compensation in 350 Line
08h	Enable Vertical Text Compensation in 400 Line
09h	Disable Vertical Text Compensation 400 Line
0Ah	Enable Vertical Graphics Compensation 350 Line
0Bh	Disable Vertical Graphics Compensation 350 Line
0Ch	Enable Vertical Graphics Compensation 400 Line
0Dh	Disable Vertical Graphics Compensation 400 Line
0Eh	Enable Vertical Graphics Compensation 480 Line
0Fh	Disable Vertical Graphics Compensation 480 Line
10h	Enable Vertical Graphics Compensation 600 Line
11h	Disable Vertical Graphics Compensation 600 Line

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh

005Fh	Function supported but failed
015Fh	Function supported and successful

5FA0h Extended BIOS Save/Restore State

This function returns the size of the buffer needed for saving the state of the video system. The user may specify which aspects of the video system are to be saved.

Calling Registers:

AX - 5FA0h Return Save/Restore buffer size

CX - Requested state:
- Bit 0 Video hardware state
- Bit 1 Video BIOS data state
- Bit 2 DAC state & Color Registers
- Bit 13 BitBLT Registers
- Bit 15 Extended Registers

Return Registers:

BX - Number of 64 Byte blocks required

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5FA1h Save Video State

This function saves information on the current state of the video system.

Calling Registers:

AX - 5FA1h Save Video State

CX - Save/Restore Options:
- Bit 0 Video Hardware State
- Bit 1 Video BIOS Data Areas
- Bit 2 Video DAC state and Color Registers
- Bit 13 BitBLT Registers
- Bit 15 Extended Registers

ES - Segment of Save Area

BX - Offset of Save Area

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5FA2h Restore Video State

This function restores a previous state of the video system from stored information.

Calling Registers:

AX	-	5FA2h Save Video State
CX	-	Save/Restore Options: Bit 0 Video Hardware State Bit 1 Video BIOS Data Areas Bit 2 Video DAC state and Color Registers Bit 13 BitBLT Registers Bit 15 Extended Registers
ES	-	Segment of Restore Area
BX	-	Offset of Restore Area

Return Registers:

AX	-	Return Status: Function not supported if AL != 5Fh 005Fh Function supported but failed 015Fh Function supported and successful

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CHAPTER 6 - VESA FUNCTION CALLS

6.1 VESA Extended VGA BIOS Functions

The HiQV32™ VGA BIOS provides a set of extended function calls as defined by the Video Electronics Standards Association to support Super VGA. More information about these functions can be found in the *VESA BIOS Extension Version 2.0, VESA VBE/PM, and VESA VBE/DDC* Standard documents. These function calls are implemented as interrupt 10h functions using AH = 4Fh.

Table 6-2. VESA Extended VGA BIOS Functions

AX	Function
4F00h	Return VBE Controller Information
4F01h	Return VBE Mode Information
4F02h	Set VBE Mode
4F03h	Get Current VBE Mode
4F04h	Save/Restore Video State
4F05h	Display Window Control
4F06h	Get/Set Logical Scan Line Length
4F07h	Get/Set Display Start
4F08h	Get/Set DAC Palette Format
4F09h	Get/Set Palette Data
4F0Ah	Return VBE Protected Mode Interface
4F10h	Display Power Management Extensions
4F15h	Display Data Channel Extensions

4F00h Return VBE Controller Information

This sub-function returns VBE revision and capability information of the HiQV32™ VGA system. The purpose of this function is to provide information to the calling program about the general capabilities of the installed VBE software and hardware. This function fills an information block structure at the address specified by the caller. The VbeInfoBlock size is 256 bytes for VBE 1.x, and 512 bytes for VBE 2.0.

Calling Registers:

AX - 4F00h Return VBE Controller Information

ES:DI - Pointer to buffer for the VbeInfoBlock
(VBE signatures should be set to "VBE2" when this function is called to indicate VBE 2.0 information is desired and the information block is 512 bytes in size.)

Return Registers:

AX - VESA VBE Return Status
Function not supported if AL !=4Fh
004Fh Function call successful
014Fh Function call failed
024Fh Function is not supported in current hardware configuration
034Fh Function is invalid in current video mode

The information block has the following structure:

```
VbeInfoBlock struc
    VbeSignature        db      'VESA'          ; 4 signature bytes
    VbeVersion          dw      200h            ; VESA version number 2.0
    OEMStringPtr        dd      ?               ; pointer to OEM string
    Capabilities        db      4 dup(?)        ; capabilities of the video environment
    VideoModePtr        dd      ?               ; pointer to supported VBE modes
    TotalMemory         dw      ?               ; number of 64KB memory blocks on board
    OemSoftwareRev      dw      ?               ; VBE implementation software revision
    OemVendorNamePtr    dd      ?               ; Pointer to vendor name string
    OemProductNamePtr   dd      ?               ; Pointer to product name string
    OemProductRevPtr    dd      ?               ; Pointer to product revision string
    Reserved            db      222 dup(?)      ; Reserved for VBE implementation scratch area
    OemData             db      256 dup(?)      ; Data for OEM strings
VbeInfoBlock ends
```

4F01h Return VBE Mode Information

This sub-function returns information about a specific VBE mode.

Calling Registers:

AX	-	4F01h Return VBE mode information
CX	-	Video mode number
ES:DI	-	Pointer to a 256 byte buffer for the ModeInfoBlock

Return Registers:

AX	-	See function 00h for status codes

The mode information block has the following structure:

```
ModeInfoBlock   struc
    ModeAttributes          dw      ?           ; mode attributes
    WinAAttributes          db      ?           ; window A attributes
    WinBAttributes          db      ?           ; window B attributes
    WinGranularity          dw      ?           ; window granularity
    WinSize                 dw      ?           ; window size
    WinASegment             dw      ?           ; window A start segment
    WinBSegment             dw      ?           ; window B start segment
    WinFuncPtr              dd      ?           ; pointer to window function
    BytesPerScanLine        dw      ?           ; bytes per scan line
    XResolution             dw      ?           ; horizontal resolution
    YResolution             dw      ?           ; vertical resolution
    XCharSize               db      ?           ; character cell width
    YCharSize               db      ?           ; character cell height
    NumberOfPlanes          db      ?           ; number of memory planes
    BitsPerPixel            db      ?           ; bits per pixel
    NumberOfBanks           db      ?           ; number of banks
    MemoryModel             db      ?           ; memory model type
    BankSize                db      ?           ; bank size in KB
    NumberOfImagePages      db      ?           ; Number of images
    Reserved                db      1           ; reserved for page function
    RedMaskSize             db      ?           ; size if direct color red mask in bits
    RedFieldPosition        db      ?           ; bit position of lsb of red mask
    GreenMaskSize           db      ?           ; size of direct color green mask in bits
    GreenFieldPosition      db      ?           ; bit position of lsb of green mask
    BlueMaskSize            db      ?           ; size of direct color blue mask in bits
    BlueFieldPosition       db      ?           ; bit position of lsb of blue mask
    RsvdMaskSize            db      ?           ; size of direct color reserved mask in bits
    RsvdFieldPosition       db      ?           ; bit position of lsb of reserved mask
    DirectColorModeInfo     db      ?           ; direct color mode attributes
    PhysBasePtr             dd      ?           ; physical address for linear frame buffer
    OffScreenMemOffset      dd      ?           ; pointer to start of offscreen memory
    OffScreenMemSize        dw      ?           ; amount of offscreen memory in 1K units
    Reserved                db      206 dup(?)  ; remainder of ModeInfoBlock
ModeInfoBlock   ends
```

4F02h Set VBE Mode

This sub-function sets a given VBE or VGA mode.

Calling Registers:

AX - 4F02h Set VBE video mode

BX - Bit 0-8 Video mode number
Bit 9-13 Reserved, (must = 0)
Bit 14 0 = use windowed (paged) frame buffer
1 = use linear (flat) frame buffer
Bit 15 0 = clear video memory
1 = do not clear video memory

Return Registers:

AX - See function 00h for status codes

4F03h Get Current VBE Mode

This sub-function returns the current video mode.

Calling Registers:

AX - 4F03h Get current video mode

Return Registers:

AX - See function 00h for status codes

BX - Current video mode number
Bit 0-13 mode number
Bit 14 0 = use windowed (paged) frame buffer
1 = use linear (flat) frame buffer
Bit 15 0 = clear video memory
1 = do not clear video memory

4F04h Save/Restore Video State

These sub-functions provide a mechanism for saving and restoring the video state. The functions are a superset of the three sub-functions under the standard VGA BIOS function 1Ch.

4F04h - 00h Return Save/Restore State Buffer Size

Calling Registers:

AX	-	4F04h	Save/restore video state
DL	**-**	**00h**	**Return save/restore state buffer size**
CX	-	Requested states	
		Bit 0	Save/restore video hardware state
		Bit 1	Save/restore video BIOS data state
		Bit 2	Save/restore video DAC state
		Bit 3	Save/restore extended video state

Return Registers:

AX	-	See function 00h for status codes
BX	-	Number of 64 byte blocks needed to hold the state buffer

4F04h - 01h Save Video State

Calling Registers:

AX	-	4F04h	Save/restore video state
DL	**-**	**01h**	**Save video state**
CX	-	Requested states	
		Bit 0	Save/restore video hardware state
		Bit 1	Save/restore video BIOS data state
		Bit 2	Save/restore video DAC state
		Bit 3	Save/restore extended video state
ES:BX	-	Pointer to state buffer	

Return Registers:

AX	-	See function 00h for status codes

4F04h - 02h Restore Video State

Calling Registers:

AX	-	4F04h	Save/restore video state
DL	**-**	**02h**	**Restore video state**
CX	-	Requested states	
		Bit 0	Save/restore video hardware state
		Bit 1	Save/restore video BIOS data state
		Bit 2	Save/restore video DAC state
		Bit 3	Save/restore extended video state
ES:BX	-	Pointer to state buffer	

Return Registers:

AX	-	See function 00h for status codes

4F05h Display Window Control

These sub-functions set or get the position of the specified window (page) in the video memory.

4F05h - 00h Set Video Memory Window

Calling Registers:

AX	-	4F05h	Display window control
BH	**-**	**00h**	**Set video memory window**
BL	-	Window number 00h 01h	 Window A Window B (Not supported)
DX	-	Window position in video memory (in 64 KBytes units)	

Return Registers:

AX	-	See function 00h for status codes

4F05h - 01h Get Video Memory Window

Calling Registers:

AH	-	4Fh	VESA Extended BIOS Function
AL	-	05h	Display window control
BH	**-**	**01h**	**Get video memory window**
BL	-	Window number 00h 01h	 Window A Window B (Not supported)

Return Registers:

AX	-	See function 00h for status codes
DX	-	Window position in video memory (in window granularity units)

4F06h Get/Set Logical Scan Line Length

These sub-functions set or get the length of a logical scan line.

Calling Registers:

AX	-	4F06h	Logical scan line length control
BL	**-**	**00h**	**Set logical scan line length in pixels**
	-	**01h**	**Return logical scan line length**
	-	**02h**	**Set logical scan line length in bytes**
	-	**03h**	**Get maximum scan line length**
CX	-	If BL=00h, desired scan line length in pixels If BL=02h, desired scan line length in bytes (ignored for get functions)	

Return Registers:

AX	-	See function 00h for status codes
BX	-	Bytes per scan line
CX	-	Actual pixels per scan line
DX	-	Maximum number of scan lines

4F07h Get/Set Display Start

These sub-functions set or get the pixel to be displayed in the upper left corner of the display from the logical page.

Calling Registers:

AX	-	4F07h	Display start control functions
BH	-	00h	Reserved, must be 0
BL	**-**	**00h**	**Set display start**
	-	**01h**	**Get display start**
	-	**80h**	**Set display start during vertical retrace**
CX	-	First displayed pixel in the scan line (Set only)	
DX	-	First displayed scan line (Set only)	

Return Registers:

AX	-	See function 00h for status codes
CX	-	First displayed pixel in scan line (Get only)
DX	-	First displayed scan line (Get only)

4F08h Get/Set DAC Palette Format

This function manipulates the operating mode for format of the DAC palette. Some DACs are configurable to provide 6 bits, 8 bits, or more of color definition for the red, green, and blue primary colors. The DAC palette width is assumed to be reset to the standard VGA value of 6 bits per primary color during any mode set.

Calling Registers:

AX	-	4F08h	Display start control functions
BH	-	Desired bits of color per primary (Set DAC palette format only)	
BL	-	00h	Set DAC Palette Format
	-	01h	Get DAC Palette Format

Return Registers:

AX	-	See function 00h for status codes
BH	-	Current number of bits of color per primary

4F09h Get/Set Palette Data

These functions are used to get or set the palette registers in the RAMDAC.

Calling Registers:

AX	-	4F09h	Get/Set Palette Data
BL	**-**	**00h**	**Set Palette Data**
	-	**01h**	**Get Palette Data**
CX	-	Number of palette registers to update (max 255)	
DX	-	First palette register index to update	
ES:DI	-	Table of palette values, in the following format:	
		DB	Blue Byte
		DB	Green Byte
		DB	Red Byte
		DB	Doubleword Alingment Byte

Return Registers:

AXh	-	See function 00h for status codes

4F0Ah Return VBE Protected Mode Interface

This function returns a pointer to a table that contains code for a 32-bit protected mode interface that can be either copied into local 32-bit memory space or can be executed from ROM providing the calling application sets all required selectors and I/O access correctly.

Calling Registers:

AX	-	4F0Ah Return VBE protected mode information
BL	**-**	**00h Return VBE protected mode information**

Return Registers:

AX	-	See function 00h for status codes
ES	-	Real mode segment of table
DI	-	Offset of table
CX	-	Length of table including protected mode code, in bytes

Table format:

ES:DI	Word offset in table of protected mode code for the Set Window portion of Function 05h.
ES:DI+2	Word offset in table of protected mode code for the Set Display Start portion of Function 07h.
ES:DI+4	Word offset in table of protected mode code for the Set Palette Data portion of Function 09h.
ES:DI+6	Word offset in table of a list of ports and memory locations that the calling application may need I/O privileges.
ES:DI+?	Variable length remainder of table, including code.

CHAPTER 7 - VESA EXTENSIONS

7.1 4F10h VESA VBE/PM (Display Power Management) Extensions

The VESA BIOS Extension sub-function 10h is used to implement power management services.

4F10h - 00h Report VBE/Power Management Capabilities

Calling Registers:

AX	-	4F10h Power management services
BL	**-**	**00h Report VBE/Power Management capabilities**
ES:DI	-	Null pointer, must be 0000:0000 in version 1.0, reserved for future use

Return Registers:

AX	-	See function 00h for status codes
BH	-	Power saving state signals supported by the controller: 1 = Supported, 0 = Not supported bit 0 STANDBY bit 1 SUSPEND bit 2 OFF bit 3 REDUCED ON (not supported) bits 4-7 Reserved for future use.
BL	-	VBE/PM version number: bits 0-3 Minor version number bits 4-7 Major version number
ES:DI		Unchanged

4F10h - 01h Set Display Power State

Calling Registers:

AX	-	4F10h	Power management services
BL	**-**	**01h**	**Set display power state**
BH	-	Requested power state:	
		00h	ON
		01h	STANDBY
		02h	SUSPEND
		04h	OFF
		08h	REDUCED ON (not supported)

Return Registers:

AX	-	See function 00h for status codes
BH	-	Unchanged

4F10h - 02h Get Display Power State

Calling Registers:

AX	-	4F10h	Power management services
BL	**-**	**02h**	**Get display power state**

Return Registers:

AX	-	See function 00h for status codes
BH	-	Power state currently requested by the controller:
		00h ON
		01h STANDBY
		02h SUSPEND
		04h OFF
		08h REDUCED ON

7.2 4F15h VBE/DDC (Display Data Channel) Extensions

The following functions support the VESA VBE / DDC (Display Data Channel) standard. The DDC standard defines a set of functions to retrieve the EDID (Extended Display Identification Data) structure from the display over the Display Data Channel.

The software implements two methods for retrieving this data: DDC1 and DDC2. DDC1 is a unidirectional data channel from the display to the host. DDC2 is a bi-directional data channel based on the I2C bus.

The Chips and Technologies, Inc. DDC1 implementation uses a modified VSync signal to retrieve the EDID block in about two seconds. The display is blank while the EDID block is being received. GPIO0 (pin #53) is the DDC1 data line. The VSync line is modified using register XR61. The data line is controlled through register FR0C and set through register XR63.

The Chips and Technologies, Inc. DDC2 implementation uses GPIO1 (pin #54) as a high speed clock line (SCL) to retrieve the EDID block in about one quarter of a second. The display is not blank while the EDID block is being received. GPIO0 (pin #53) is used as the DDC2 data line (SDA). The SCL and SDA lines are controlled through register FR0C and set through register XR63.

4F15h - 00h Report DDC Capabilities

Calling Registers:

AX	-	4F15h	VBE/DDC management services
BL	**-**	**00h**	**Report DDC Capabilities**
CX	-	00h	Controller unit number (00 = primary controller)
ES:DI		Null pointer, must be 0:0 in version 1.0. Reserved for future use.	

Return Registers:

AX	-	See function 00h for status codes		
BH	-	Approximate time in seconds, rounded up to transfer one EDID block (128bytes).		
BL	-	DDC level supported by both the display and the controller:		
		Bit 0	0	DDC1 not supported
			1	DDC 1 supported
		Bit 1	0	DDC2 not supported
			1	DDC2 supported
		Bit 2	0	Screen not blanked during data transfer.
			1	Screen blanked during data transfer.
CX	-	Unchanged		
ES:DI	-	Unchanged		

4F15h - 01h Read EDID

Calling Registers:

AX	-	4F15h	VBE/DDC management services
BL	**-**	**01h**	**Read EDID**
CX	-	00h	Controller unit number (00 = primary controller)
ES:DI			Pointer to area in which the EDID block (128 bytes) shall be returned.

Return Registers:

AX	-	See function 00h for status codes
BH	-	Unchanged
CX	-	Unchanged
ES:DI	-	Pointer to area in which the EDID block is returned

CHAPTER 8 - HOOKS FOR THE SYSTEM BIOS

8.1 INT 15h / INT 42h Hooks for the System BIOS

The video BIOS performs several interrupt function calls (interrupt 15h / 42h hooks). Each function provides the system BIOS with the opportunity to gain control at specific times to perform any custom processing that may be required. After each interrupt hook, the system BIOS must return control to the video BIOS. These hooks can be BMPed to disabled, use interrupt 15h, or use interrupt 42h. Interrupt 42h is given as an option because of the growing unreliability on interrupt 15h to return register data. These functions are implemented at the discretion of the system BIOS designer. Table 8-1 shows the hooks for the system BIOS.

Table 8-1. INT 15h/INT 42h Hooks for the System BIOS

AX	Function	Hook (INT) / BMP option
5F31h	POST Completion Notification Hook	Disabled, Int 15h, or Int 42h
5F33h	Hook After Mode Set	Disabled, Int 15h, or Int 42h
5F35h	Monitor Sensing Hook	Disabled, Int 15h, or Int 42h
5F36h	Set NTSC / PAL Hook	Disabled, Int 15h, or Int 42h
5F38h	Hook Before Mode Set	Disabled, Int 15h, or Int 42h
5F40h	Set Panel Type Hook	Disabled, Int 15h, or Int 42h
5F42h	3.3V / 5.0V Power Switching Hook	Disabled, Int 15h, or Int 42h
5F45h	Hook VESA VBE / DDC Functions	Disabled, Int 15h, or Int 42h
5F46h	Hook VESA VBE / PM Functions	Disabled, Int 15h, or Int 42h
5F47h	Notify Display Switch Hook	Disabled, Int 15h, or Int 42h
5F48h	VESA DDC Read & Write Function Hooks	Disabled, Int 15h, or Int 42h

5F31h POST Completion Notification Hook

This hook signals the completion of video POST (Power On Self Test). The hook executes just before the sign-on message is displayed, allowing the system BIOS to switch to a different display before attempting to display the sign-on message.

Calling Registers:

AX - 5F31h POST Completion Notification Hook

Return Registers:

None

5F33h Hook After Mode Set

This hook allows the system BIOS to intercept the video BIOS at the end of a mode set.

Calling Registers:

AX - 5F33h Hook after Mode Set

BH - Number of character columns

BL - Current mode number

CH - Active display page

Return Registers:

None

5F35h Video Display Hook

This hook allows the system BIOS to perform monitor sensing and to override the video display setting in the BMP. The video BIOS will set the returned video display (CRT, flat panel, or simultaneous) upon exiting video.

Calling Registers:

AX - 5F35h Video Display Hook

DL - Invalid return code

Return Registers:

DL - If unchanged, boot according to the BMP setting
- If changed, boot from the following display:
  - 00h Set to CRT display mode
  - 01h Set to flat panel display mode
  - 02h Set to simultaneous display mode

5F36h Set NTSC / PAL Hook

This hook notifies the system BIOS of the NTSC or PAL state that is about to be set.

Calling Registers:

AX	-	5F36h Set NTSC / PAL Hook
BH	-	NTSC / PAL State being set: 00h Disable NTSC and PAL 01h Enable NTSC 02h Enable PAL

Return Registers:

None

5F38h Hook Before Mode Set

This hook allows the system BIOS to intercept the video BIOS before setting the mode.

Calling Registers:

AX	-	5F38h Hook before Mode Set
CL	-	New Video Mode To Be Set

Return Registers:

None

5F40h Set Panel Type Hook

This hook allows the system BIOS to select one of eight LCD panel types upon power up (see Table 8-2).
A value of 0 in CL corresponds to Panel Type #1. 40K BIOS supports 8 panels and 44K BIOS supports 16 panels.

Table 8-2: Panel Types

Panel #	Panel Type
1	1024x768 Dual Scan STN Color Panel
2	1280x1024 TFT Color Panel
3	640x480 Dual Scan Color Panel
4	800x600 Dual Scan Color Panel
5	640x480 Sharp TFT Color Panel
6	640x480 18-bit TFT Color Panel
7	1024x768 TFT Color Panel
8	800x600 TFT Color Panel
9	800x600 TFT Color Panel (44K BIOS only)
10	800x600 TFT Color Panel (44K BIOS only)
11	800x600 Dual Scan Color Panel (44K BIOS only)
12	800x600 Dual Scan Color Panel (44K BIOS only)
13	1024x768 TFT Color Panel (44K BIOS only)
14	1024x768 TFT Color Panel (44K BIOS only)
15	Reserved
16	Reserved

Calling Registers:

AX - 5F40h Set Panel Type Hook

CL - 55h

Return Registers:

CL - 0 - 7 (panel type)

5F42h 3.3V/5.0V Power Switching-(Dual Power Supply Systems)

This hook allows the system BIOS to switch between a 3.3 volt and a 5.0 volt power supply.

Calling Registers:

AX	-	5F42h	3.3/5.0V Power Switching Hook
BH	-	Desired Voltage Switch	
		00h	Switch from 5.0 volts to 3.3 volts
		01h	Switch from 3.3 volts to 5.0 volts
		02h	Desire to switch to 5.0 volts
BL	-	55h	Is 5.0 volt level available?

Return Registers:

BL	-	Return Status:	
		01h	Hook supported and switch successful
		00h	Hook supported, but switch unsuccessful
		55h	Hook not supported

5F45h Hook for VESA VBE/DDC Functions

This hook allows the system BIOS to initialize data before or take over the VESA VBE / DDC (Display Data Channel) functions. The video BIOS DDC functions are executed if a 5Fh is not returned in AL or if AH is greater than 01h. The system BIOS must return the correct DDC function status in AH when 5Fh is returned in AL. This status will be converted into VESA VBE / DDC function status.

Calling Registers:

AX	-	5F45h	Hook VESA VBE/DDC Functions

Return Registers:

AX	-	Return Status:	
		Function not supported if AL != 5Fh	
		005Fh	Function supported but failed
		015Fh	Function supported and successful
		025Fh-FF5Fh	Function was successful, but run video BIOS DDC functions

5F46h Hook for VESA VBE/PM Functions

This hook allows the system BIOS to initialize data before, or take over the Video BIOS VESA VBE / PM (Monitor Power Management) functions. The video BIOS PM functions are executed if a 5Fh is not returned in AL or if AH is greater than 01h. The system BIOS must return the correct PM function status in AH when 5Fh is returned in AL. This status will be converted into VESA VBE/PM function status.

Calling Registers:

AX - 5F46h Hook for VESA VBE/PM Functions
BL - VESA PM Sub Function Number
- 00h Report VBE/PM services
- 01h Set display power state
- 02h Set display power state

Return Registers:

AX - Return Status:
Function not supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful
- 025Fh-FF5Fh Function was successful, but run video BIOS PM functions

5F47h Notify Display Switch Hook (CRT,FlatPanel,Simultaneous)

This hook will notify the system BIOS that a possible display switch has taken place (i.e. function 5F51h). It will offer the current new display type as an input. The purpose of this hook is to inform the system BIOS to activate or deactivate hardware used by certain displays (i.e. back light or digitizer for flat panels).

Calling Registers:

AX - 5F47h Notify Display Switch Hook

BL - Display Type
- 00h CRT display
- 01h Flat panel display
- 02h Simultaneous display

Return Registers:

AX - Return Status:
Function supported if AL != 5Fh
- 005Fh Function supported but failed
- 015Fh Function supported and successful

5F48h VESA VBE/DDC Read and Write Functions Hook

This hook allows a system with a unique hardware VESA VBE / DDC (Display Data Channel) design to use the bulk of the video BIOS's DDC code. It does this by calling the system BIOS with sub-functions (sub-hooks) that will read and write the DDC data lines, read and write the DDC clock lines, and initialize and restore the DDC state.

NOTES: The BMP utility must be used to active this hook and the DDC1 or DDC2 functionality. If this hook is implemented totally, it is not important which GPIO pin is selected for DDC1 or DDC2. The initialize and reset sub-hooks should return AL = 5Fh (System BIOS Support) even if no initialization is needed in order to stop unwanted initialization due to the GPIO pin selected.

5F48h - 00h Read DDC Data Line Sub-hook

This sub-hook calls the system BIOS to read and return the current level of the DDC1 or DDC2 data line. The video BIOS read DDC data line function is executed if a 5Fh is not returned in AL.

Calling Registers:

AX	-	5F48h	DDC Read and Write Functions Hook
BH	-	00h	Read DDC Data Line Sub-hook

Return Registers:

AL	-	5Fh	System BIOS Support
BL	-	DDC Data Line Level:	
		00h	Data line is low
		01h	Data line is high

5F48h - 01h Write DDC Data Line Sub-hook

This sub-hook calls the system BIOS to write a given level to the DDC1 or DDC2 data line. The video BIOS write DDC data line function is executed if a 5Fh is not returned in AL.

Calling Registers:

AX	-	5F48h	DDC Read and Write Functions Hook
BH	-	01h	Write DDC Data Line Sub-hook
BL	-	DDC Data Line Level:	
		00h	Set data line low
		01h	Set data line high

Return Registers:

AL	-	5Fh	System BIOS Support

5F48h - 02h Read DDC2 Clock Line Sub-hook

This sub-hook calls the system BIOS to read and return the current level of the DDC2 clock line. The video BIOS read DDC2 clock line function is executed if a 5Fh is not returned in AL.

Note: This sub-hook must not change the clock line direction from an output to an input. This action may cause clock line noise and bad EDID data.

Calling Registers:

AX	-	5F48h	DDC Read and Write Functions Hook
BH	-	02h	Read DDC2 Clock Line Sub-hook

Return Registers:

AL	-	5Fh	System BIOS Support
BL	-	DDC2 Clock Line Level:	
		00h	Clock line is low
		01h	Clock line is high

5F48h - 03h Write DDC2 Clock Line Sub-hook

This sub-hook calls the system BIOS to write a given level to the DDC2 clock line. The video BIOS write DDC2 clock line function is executed if a 5Fh is not returned in AL.

Calling Registers:

AX	-	5F48h	DDC Read and Write Functions Hook
BH	-	03h	Write DDC2 Clock Line Sub-hook
BL	-	DDC2 Clock Line Level:	
		00h	Set clock line low
		01h	Set clock line high

Return Registers:

AL	-	5Fh	System BIOS Support

5F48h - 04h Initialize Before DDC Functions Sub-hook

This sub-hook calls the system BIOS to initialize the system state if necessary before the DDC functions are executed. The video BIOS initialize state before DDC function is executed if a 5Fh is not returned in AL.

Note: This sub-hook is also call in video POST.

Calling Registers:

AX	-	5F48h	DDC Read and Write Functions Hook
BH	-	04h	Initialize Before DDC Functions Sub-hook

Return Registers:

AL	-	5Fh	System BIOS Support

5F48h - 05h Reset After DDC Functions Sub-hook

This sub-hook calls the system BIOS to reset the system state if necessary after the DDC functions have executed. The video BIOS reset state after DDC function is executed if a 5Fh is not returned in AL.

Calling Registers:

AX	-	5F48h	DDC Read and Write Functions Hook
BH	-	05h	Reset After DDC Functions Sub-hook

Return Registers:

AL	-	5Fh	System BIOS Support

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CHAPTER 9 - OEM UTILITY PROGRAMS

The OEM utility programs allow the OEM to prepare the 65550 BIOS for use. The BMP utility program enables the OEM to prepare a custom version of the BIOS.

Note:	The OEMs may not reproduce nor distribute these programs.

9.0. BMP

The BMP550 enables OEMs to customize the 65550 BIOS for their own specific requirements. The BMP allows the OEM to modify certain parameters of a binary version of the BIOS to be modified. The parameters that the BMP can modify include:

- Sign-on message
- General and flat panel BIOS Features
- Display type determination
- Set FP Dot Clock
- Set FP Memory Clock
- Extended display modes
- 65550 register tables

The BMP may only be used once on a copy of the BIOS. The OEM should make a backup copy of the original diskette(s) before using any of the OEM utilities. Once the BIOS is changed and saved from the BMP, it cannot be modified again.

9.1. Usage

```
BMP550 [File]
```

`[File]` Optional filename of the BIOS file input to the BMP. A default extension of .DAT is assumed if no extension is specified. A default filename of VGA550.DAT is assumed if no filename is specified.

9.2. Filenames

Default filenames for the 65550 BIOS are:

- `BMP550.EXE`
- `VGA550.DAT`
- `RAM550.DAT`

9.3. Examples

ROM Binary:

```
BMP550 [VGA550.DAT]
```

Executes BMP550 with the default file VGA550.DAT as the input file.

RAM Executable:

```
BMP550 RAM550.EXE
```

Executes BMP550 with the RAM550.EXE or utility program as the input file.

9.4. Commands

BMP550 organizes the modifiable parameters of the 65550 BIOS into several windows. Some values are entered as text or as hexadecimal values within these windows. The following keys are used to change fields or edit values:

<Tab>	Go to next window.
<Shift Tab>	Go to previous window.
<PgUp>	Move up one page within a window.
<PgDn>	Move down one page within a window.
<↑>,<↓>	Move up or down one line or field.
<←>,<→>	Move left or right one character or field.
<+>,<->	Enable/disable parameter. Increment/decrement a value in the field.
<F1>	Help.
<F5>	Save BMS file.
<F6>	Load BMS file.
<F10>	Save changes to the BIOS file.
<Esc>	Exit program.

9.5. Help

Help messages can be displayed by moving to the parameter that requires further explanation and pressing the <F1> key. A pop-up window will be displayed describing the parameter.

9.6. BMS Files

BMP550 provide the capability to save and load custom files (BMS Files) that contain all of the 65550 BIOS parameters that can be modified. There is no limit to the number of custom files that user may save.

9.7. Error Messages

If BMP550 encounters an error during operation, a red window will appear which will contain the error condition. Table 9-1 lists these errors, the possible cause, and recommended solution.

Table 9-1: BMP550 Error Messages.

Error Message	Problem Description, Recommended Action
Use original BIOS file	The file has already been modified and saved. Use the binary file that was supplied on the original disk. If this does not work, contact local CHIPS sales representative.
Editable Structure not found	The file can not be modified. This is the wrong file. The binary file that was supplied on the original disk should be used.
This program is unable to edit the BMP structure in that file	There is an incompatible version of BMP and binary file. Use the binary file and BMP program supplied on the original disk.
Bad BMP structure, Old version was Num, header version was Num	This is an incompatible version of BMP or binary file. Use the binary file and BMP program supplied on original disk.
Unable to allocate memory	There is not enough system memory. Remove all unnecessary resident programs and reboot the system. BMP requires approximately 300K of memory.
Binary file File not found	BMP could not find the specified file. Verify that the specified file exists.
Unable to read binary file File	BMP could not read the specified file. Specified file may be corrupted, use backup copy.
Unable to write to File	There was an error during write to specified file. The file may be marked read-only. Try making changes to a file that has read and write access.
Unable to reopen File for saving	Unable to re-open binary file. The file may be a read-only file. Try making changes to a file with read and write access.
Unable to open my own .EXE file File	Unable to open BMP550.exe for reading. This may be due to insufficient memory, or because the BMP550.exe filename has been changed. Use the BMP and binary files from the original disk.
Unable to open BMS file BMSfile	Unable to find or read BMS file. Try specifying a file that does exist.
Unable to create file BMSfile	Unable to write a BMS file. There may be insufficient disk space, or an existing file has read-only access.

Note:

File	Binary filename used.
Num	Version number of BMP structure in BMP and/or binary file.
BMSfile	BMS filename used.

9.8. Message Options

The figure below shows a sample BMP frame.

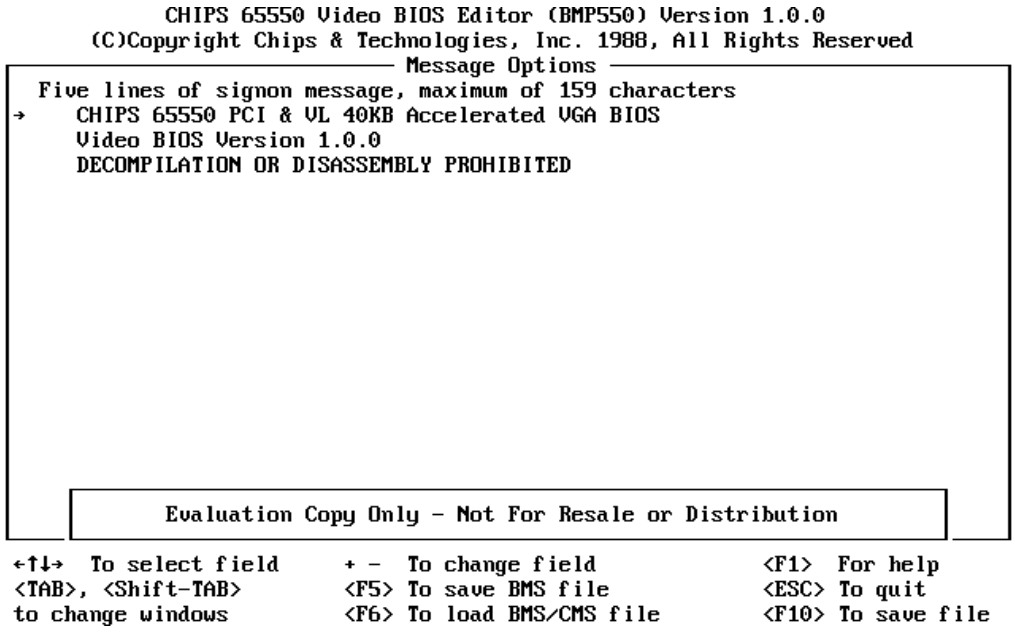

Figure 1: Sample BMP Frame

Previous CHIPS OEM reference guides displayed a sample of each different frame. This reference guide shows only the one sample above and presents the content of the frames through a series of tables. Each table corresponds to one screen of the BMP editor. Each table lists the title of each field, provides a description of the field, and provides the possible values for each field. The default values appear in **bold** text.

The BMP frames are a set of windows that allows the OEM to adjust the CRT register values for all extended modes. In addition, the dot clock frequency can be specified for each mode (except modes 60 and 61). There is one screen for each distinct table of CRT register values that the video BIOS uses. Often, more than one mode uses a table, and the dot clock frequencies can be set separately for each of these modes. These BMP pages are not reflected in the following tables.

The following pages have several tables. The tables list: the panel types, the BMP screens and their functions, and the individual field definitions for each BMP screen.

9.9. Built in Panel Support

The sixteen panels supported are as follows:

Table 9-2: Panel Types

Panel #	Panel Type
1	1024x768 Dual Scan STN Color Panel
2	1280x1024 TFT Color Panel
3	640x480 Dual Scan Color Panel
4	800x600 Dual Scan Color Panel
5	640x480 Sharp TFT Color Panel
6	640x480 18-bit TFT Color Panel
7	1024x768 TFT Color Panel
8	800x600 TFT Color Panel
9	800x600 TFT Color Panel (44K BIOS only)
10	800x600 TFT Color Panel (44K BIOS only)
11	800x600 Dual Scan Color Panel (44K BIOS only)
12	800x600 Dual Scan Color Panel (44K BIOS only)
13	1024x768 TFT Color Panel (44K BIOS only)
14	1024x768 TFT Color Panel (44K BIOS only)
15	Reserved
16	Reserved

The table below lists the pages of the BMP utilities and their functions. The tables in the remainder of this chapter provides a description of each field on each frame and the default values of each field.

Table 9-3: BMP Screens and Functions

Screen Number	Function
Page: 1	Message Options
Pages: 2-3	BIOS Features
Page 4	ENABLE/DISABLE MODES
Pages: 5-7	CRT Boot parameters (XR); FP & SM Boot Parameters (FR); MM Boot Parameters (MR)
Page: 8	CRT & Panel Switch parameters
Page: 9	Panel#1 Flat Panel and Simultaneous video parameters:
Pages: 10 - 12	Panel#1: Control Parameters, Flat Panel Parameters, Simultaneous video parameters (FR)
Page: 13	Panel#2 Flat Panel and Simultaneous video parameters:
Pages: 14-16	Panel#2 Control Parameters (FR); Flat Panel Parameters (FR); Simultaneous video parameters (FR)
Page: 17	Panel#3 Flat Panel and Simultaneous video parameters:
Pages: 18-20:	Panel#3 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 21	Panel#4 Flat Panel and Simultaneous video parameters:
Pages: 22-24	Panel#4 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 25	Panel#5 Flat Panel and Simultaneous video parameters:
Pages: 26-28	Panel#5 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 29	Panel#6 Flat Panel and Simultaneous video parameters:
Pages: 30-32	Panel#6 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 33	Panel#7 Flat Panel and Simultaneous video parameters:
Pages: 34-36	Panel#7 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 37	Panel#8 Flat Panel and Simultaneous video parameters:
Pages: 38-40	Panel#8 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 42	Panel#9 Flat Panel and Simultaneous video parameters:
Pages: 43-45	Panel#9 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)

Table 9-3: BMP Screens and Functions (continued)

Screen Number	Function
Page: 46	Panel#10 Flat Panel and Simultaneous video parameters:
Pages: 47-49	Panel#10 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 50	Panel#11 Flat Panel and Simultaneous video parameters:
Pages: 51-53	Panel#11 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 54	Panel#12 Flat Panel and Simultaneous video parameters:
Pages: 55-57	Panel#12 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 58	Panel#13 Flat Panel and Simultaneous video parameters:
Pages: 59-61	Panel#13 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 62	Panel#14 Flat Panel and Simultaneous video parameters:
Pages: 63-65	Panel#14 Control Parameters (FR); Flat Panel PARAMETERS (FR); Simultaneous video parameters (FR)
Page: 66	Panel#15 Reserved
Page: 70	Panel#16 Reserved

Table 9-4: BMP Page 1
Message Options

Title	Description	Value
Five lines of sign-on message, maximum of 159 characters	**CHIPS 65550 VGA PCI & VL Accelerated VGA BIOS** This is the sign-on message that will be displayed when the machine is booted. You may enter a maximum of five lines of text, with no more than 70 characters on each line, and no more than 159 total characters.	N/A

Table 9-5: BMP Page 2
BIOS Features

Title	Description	Value
General Features		
	Popup Support	**Disabled** / Enabled
	Adjust Popup Position if Popup is used	**Yes** No
	Total Number Of Popup	**1**, 2, 3, 4, 5, 6, 7, 8
	Set DDC2 Clock Line GPIO pin DDC1 implementations should set this entry to disabled. If a DDC line will use GPIO 1 or GPIO 0, FR0C should set that GPIO pin as an input. (See the FP & SM Boot Parameters page.)	GPIO 0 GPIO 1 GPIO 2 (PCI bus only) GPIO 3 **BIOS DDC2 Disabled**
	Set DDC1 or DDC2 Data Line GPIO pin If this entry is set to BIOS DDC1 and DDC2 Disabled, both DDC1 and DDC2 will be disabled. However, DDC dispatching and the system BIOS interrupt hook will continue to take place. If a DDC line will use GPIO 1 or GPIO 0, FR0C should set that GPIO pin as an input.(See the FP & SM Boot Parameters page.)	GPIO 0 GPIO 1 GPIO 2 (PCI bus only) GPIO 3 **BIOS DDC1 and DDC2 Disabled**
	Enable/Disable Voltage Switching	**Disabled** Enabled
	Perform DAC test during initialization If set to 'NO' the DAC test will not be performed, and therefore no DAC errors will be reported. This is useful for systems with no DAC. If set to 'YES' (default), the DAC will be tested.	**Yes** No
	ROM Segment This is the code segment at which the BIOS will run. The segment of an AT adapter board BIOS is usually C000h. The segment of a motherboard BIOS is not specifically defined, and varies from board to board. C000h and E000h are typical.	**C000**, C800, D000, D800, E000, E800, F000, F800
	VESA VBE/PM Implementation The VESA VBE/PM implementation will change when the (Use Panel Off State) selection is chosen. With this selection, all PM states, except for the on state will use the CHIPS panel off mode. This will help save laptop battery power.	**Normal** Use Panel Off State

Table 9-5: BMP Page 2 (continued)
BIOS Features

Title	Description	Value
5.0V CRT Display Memory Clock Frequencies:		
	Standard VGA Modes	25-40 MHz **Default 40MHz**
	640x480 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	640x480 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	640x480 24 Bpp modes	25-40 MHz **Default 40MHz**
	800x600 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	800x600 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	800x600 24 Bpp modes	25-40 MHz **Default 40MHz**
	1024x768 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	1024x768 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	1024x768 24 Bpp modes	25-40 MHz **Default 40MHz**
	1280x1024 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	1280x1024 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	1280x1024 24 Bpp modes	25-40 MHz **Default 40MHz**

Table 9-5: BMP Page 2 (continued)
BIOS Features

Title	Description	Value
3.3V CRT Display Memory Clock Frequencies:		
	Standard VGA Modes	25-40 MHz **Default 40MHz**
	640x480 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	640x480 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	640x480 24 Bpp modes	25-40 MHz **Default 40MHz**
	800x600 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	800x600 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	800x600 24 Bpp modes	25-40 MHz **Default 40MHz**
	1024x768 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	1024x768 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	1024x768 24 Bpp modes	25-40 MHz **Default 40MHz**
	1280x1024 4/8 Bpp modes	25-40 MHz **Default 40MHz**
	1280x1024 15/16 Bpp modes	25-40 MHz **Default 40MHz**
	1280x1024 24 Bpp modes	25-40 MHz **Default 40MHz**
General Features		
	Video Memory Type	**User Defined** Hardware Defined
	Video Memory Size	**Auto** User Defined

Table 9-6: BMP Page 3
BIOS Features

Title	Description	Value
Bus Features		
	Set Bus Type	**PCI,** VL
	Video Linear Start High Address in MB (VL-Bus only) This allows to set Video Linear Start Address in Linear Graphics Modes. Hardware also needs to be set for this address.	0, 16, **32**, 48, 64, 80, 96, 112, 128
	Video Linear Start Low Address in MB (VL-Bus only)	**0,** 8
Display Determination:		
	Analog Display Boot Type This selects the boot display type - CRT, FP or Simultaneous	**Analog Display Type Override** Auto Boot On FP Or Simultaneous Auto Boot On FP Or CRT
	Analog Display Boot Type Override	Use override **Simultaneous boot** FP boot CRT boot"
Panel Type:		
	Read Switches	**No**, Yes
	Select Panel If Panel is selected based on BMP then this field will be used to set the Panel type.	PANEL#1 1024x768 Dual Scan Color PANEL#2 1280x1024 TFT Color PANEL#3 640x480 Dual Scan STN Color PANEL#4 800x600 Dual Scan STN Color PANEL#5 640x480 Sharp TFT Color **PANEL#6 640x480 18-Bit TFT Color** PANEL#7 1024x768 TFT Color PANEL#8 800x600 TFT Color PANEL#9 800x600 TFT Color (44K BIOS only) PANEL#10 800x600 TFT Color (44K BIOS only) PANEL#11 800x600 Dual Scan Color (44K BIOS only) PANEL#12 800x600 Dual Scan Color (44K BIOS only) PANEL#13 1024x768 TFT Color (44K BIOS only) PANEL#14 1024x768 TFT Color (44K BIOS only) PANEL#15 Reserved PANEL#16 Reserved

Table 9-6: BMP Page 3 (continued)
BIOS Features

Title	Description	Value
System BIOS Hooks		
	Set Panel Type Hook The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	Disabled **USE INT 15H** USE INT 42H
	Hook Before Mode Set The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	**Disabled** USE INT 15H USE INT 42H
	Hook After Mode Set The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	**Disabled** USE INT 15H USE INT 42H
	POST Completion Hook The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	Disabled **USE INT 15H** USE INT 42H
	Boot Up Display Type Hook (CRT, Panel, Simultaneous) The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	Disabled **USE INT 15H** USE INT 42H
	Notify Display Switch Hook (CRT, Panel, Simultaneous) The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	**Disabled** USE INT 15H USE INT 42H
	3.3/5.0 volt Power Switching Hook The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	Disabled **USE INT 15H** USE INT 42H

Table 9-6: BMP Page 3 (continued)
BIOS Features

Title	Description	Value
System BIOS Hooks		
	Hook Before VESA VBE/DDC The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	**Disabled** USE INT 15H USE INT 42H
	VESA VBE/DDCRead and Write Functions Hook The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	**Disabled** USE INT 15H USE INT 42H
	Hook Before VESA VBE/PM The video BIOS will call interrupt 15h, interrupt 42h, or no interrupt as requested. Interrupt 42h is made available because interrupt 15h is becoming less reliable.	**Disabled** USE INT 15H USE INT 42H

Table 9-7: BMP Page 4
ENABLE/DISABLE MODES

Title	Description	Value
CRT Display Mode		Binary Defaults:
58, 54, 52, 50, 48/49, 46,	Enable/Disable CRT Interlaced Modes 5V	**1100 1010 0010 1000**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable CRT Interlaced Modes 3V	**1100 1010 0010 1000**
36, 34, 32, 31, 30	Enable/Disable CRT 56Hz Modes in 5V	**0011 0001 0000 0100**
	Enable/Disable CRT 56Hz Modes in 3V	**0010 0001 0000 0100**
	Enable/Disable CRT 60Hz Modes in 5V	**1111 1111 1111 1101**
	Enable/Disable CRT 60Hz Modes in 3V	**1111 1111 1111 1101**
	Enable/Disable CRT 75Hz Modes in 5V	**1111 1011 1010 1101**
	Enable/Disable CRT 75Hz Modes in 3V	**0111 0011 1000 1101**
	Enable/Disable CRT 85Hz Modes in 5V	**0111 0011 1000 1101**
	Enable/Disable CRT 85Hz Modes in 3V	**0111 0011 1000 1101**
PNL#1 1024x768 Dual Scan		Binary Default:
Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#2 1280x1024 TFT Color		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#3 640x480 Dual Scan		Binary Default:
STN Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#4 800x600 Dual Scan		Binary Default:
STN Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#5 640x480 Sharp TFT		Binary Default:
Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#6 640x480 18-Bit TFT		Binary Default:
Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#7 1024x768 TFT Color		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#8 800x600 TFT Color		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**

Table 9-7: BMP Page 4 (continued)
ENABLE/DISABLE MODES

Title	Description	Value
PNL#9 800x600 TFT Color		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#10 800x600 TFT Color		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#11 800x600 Dual Scan		Binary Default:
STN Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#12 800x600 Dual Scan		Binary Default:
STN Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#13 1024x768 TFT		Binary Default:
Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#14 1024x768 TFT		Binary Default:
Color	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#15 Reserved		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**
PNL#16 Reserved		Binary Default:
58, 54, 52, 50, 48/49, 46,	Enable/Disable SM Modes in 5V	**1111 1111 1111 1111**
44/45, 42/43, 40/41, 3A, 38,	Enable/Disable SM Modes in 3V	**1111 1111 1111 1111**
36, 34, 32, 31, 30	Enable/Disable FP Modes in 5V	**1111 1111 1111 1111**
	Enable/Disable FP Modes in 3V	**1111 1111 1111 1111**

Note: Panels #9 - #16 are available only in 44K BIOS.

Table 9-7: BMP Page 5

NTSC / PAL Mode 3+ Clock and CRT parameters

Title	Description	Value
Clock M Value = XRC8 + 2, Clock N Value = XRC9 + 2		
Title CRT Indexes = 00 01 02 03 04 05 06 07 09 10 11 12 13 15 16		
	Activate NTSC / PAL Support in Applications	**Disabled** Enabled
Mode 3 + NTSC-Clock M, N		Two Hex Characters **40 41**
	CRT Values	15 hex characters **6B 4F 50 8B 5B 83 03 11 47 E1 99 C7 28 DE EB**
Mode 3 + PAL-Clock M, N		Two Hex Characters **2C 2D**
	CRT Values	15 hex characters **6B 4F 50 8B 5B 83 36 11 47 FB 93 C7 28 F8 05**
Mode 13 NTSC-Clock M, N		Two Hex Characters **40 41**
	CRT Values	15 hex characters **6B 4F 50 8B 5B 83 03 11 40 E1 99 C7 28 DE EB**
Mode 13 PAL-Clock M, N		Two Hex Characters **2C 2D**
	CRT Values	15 hex characters **6B 4F 50 8B 5B 83 36 11 40 FB 93 C7 28 F8 05**
Mode 640x480 NTSC - Clock M, N		Two Hex Characters **40 41**
	CRT Values	15 hex characters **6B 4F 50 8B 5B 83 03 11 40 F5 D9 EF 50 F3 02**
Mode 640x480 PAL - Clock M, N		Two Hex Characters **2C 2D**
	CRT Values	15 hex characters **6B 4F 50 8B 5B 83 2D 1D 40 0F 97 EF 50 A0 19**

Table 9-8: BMP Page 6
CRT Boot parameters (XR)

Title	Description	Value
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

Table 9-9: BMP Page 7
FP & SM Boot Parameters (FR)

Title	Description	Value
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

Table 9-10: BMP Page 8
MM Boot Parameters (MR)

Title	Description	Value
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

Table 9-11: BMP Page 9
CRT & Panel Switch parameters

Title	Description	Value
CRT Switch Parameters (XR) FP & SM Switch Parameters (FR)		
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

Note: The standard 65550 BIOS supports 16 panel types as shown in Table 9-2 of section 5.1.9 and at the end of this section. The following pages are an example of one flat panel type. All 16 flat panel modes will have the same layout as this example.

Table 9-12: BMP Page 10

Panel#1 Flat Panel and Simultaneous video parameters

Title	Description	Value
Panel Configuration:		
	Panel Type	**1024x768 Dual Scan Color STN**
Video Memory Selections:		
	Type (if User Defined in General Features) This will set video memory type for Panel #1 if 'User Defined' is selected for 'Video memory type' under 'General Features'.	Conventional (FPM) **Ext Data Out (EDO)**
	Size (if User Defined in General Features) This will set video memory size for Panel #1 if 'User Defined' is selected for 'Video memory size' under 'General Features'.	**1 MB** 2 MB
Flat Panel Display Mode Clock Frequencies:		
Flat Panel Mode (5V):	Std/4/8 Bpp Dot Clock	6 - 135 MHz Default: **44MHz**
	15/16 Bpp Dot Clock	6 - 135 MHz Default: **44MHz**
	24 Bpp Dot Clock	6 - 135 MHz Default: **44MHz**
	Std/4/8 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	15/16 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	24 Bpp Memory Clock	6 - 135 MHz Default: **49MHz**
Flat Panel Mode (3.3V):	Std/4/8 Bpp Dot Clock	6 - 135 MHz Default: **46MHz**
	15/16 Bpp Dot Clock	6 - 135 MHz Default: **44MHz**
	24 Bpp Dot Clock	6 - 135 MHz Default: **44MHz**
	Std/4/8 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	15/16 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	24 Bpp Memory Clock	6 - 135 MHz Default: **49MHz**

Table 9-12: BMP Page 10 (continued)

Panel#1 Flat Panel and Simultaneous video parameters

Title	Description	Value
Simultaneous Display Mode Clock Frequencies:		
Flat Panel Mode (3.3V):	Dot Clock	6 - 135 MHz Default: **65MHz**
	Std/4/8 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	15/16 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	24 Bpp Memory Clock	6 - 135 MHz Default: **49MHz**
Flat Panel Mode (5V):	Dot Clock	6 - 135 MHz Default: **46MHz**
	Std/4/8 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	15/16 Bpp Memory Clock	6 - 135 MHz Default: **40MHz**
	24 Bpp Memory Clock	6 - 135 MHz Default: **49MHz**

Table 9-13: BMP Page 11 Panel#1: Control Parameters		
Title	**Description**	**Value**
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

Table 9-14: BMP Page 12 Panel#1: Flat Panel Parameters		
Title	**Description**	**Value**
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

Table 9-15: BMP Page 13 Panel#1: Simultaneous video parameters		
Title	**Description**	**Value**
	Extended registers (address, data)	Data listed is two hexadecimal values. The first is the extension register address. The second is the value of the register.

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APPENDIX A - BUILDING THE VGA BIOS

This appendix describes the process for creating a binary BIOS from source code. Building, modifying, or updating the BIOS Source Code requires the following software utilities:

- A text editor capable of editing ASCII files
- Microsoft Macro Assembler (MASM) version 5.10 or 6.11
- Microsoft Linker (LINK) version 5.31
- Microsoft MAKE utility

The INSTALL.BAT file on the source code diskette will install all the files necessary to create a binary version of the BIOS. Use the following command line to install:

```
A:INSTALL C:\VGA550
```

INSTALL.BAT will create the directory \VGA550 on drive C:. The following subdirectories will also be created:

```
\OBJ
\LST
```

The BIOS source files will be placed in the \VGA550 or directory, along with batch files for assembling and linking the BIOS. INSTALL.BAT will then copy the binary files into the \OBJ subdirectory.

To create the binary copy of the BIOS, run the Microsoft Make utility with the following command line:

```
MAKE MAKEFILE
```

or use

```
MKB550.bat
```

Note: Several "warning" messages may appear while Make is assembling certain source modules. These warning messages should be ignored. However, there should be no "error" messages from the assembler.

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APPENDIX B - Suspend/Resume Procedure

B 1.0 Introduction

The following section describes the Suspend/Resume procedure required for the Chips and Technologies, Inc. HiQV32™ (65550) High Performance Flat Panel/CRT VGA Controller.

Following this procedure will allow the 65550 to perform optimally during Suspend/Resume operations. Ignoring this procedure will result in rare intermittent failures during Suspend/Resume operations. Chips and Technologies, Inc. cannot be responsible for the operation of the 65550 during Suspend/Resume if this procedure is not properly followed.

This section contains brief description of the procedure followed by an example code. The actual method that implements this Suspend/Resume procedure depends on the system logic chip set as well as the power management software. Please remember that it is only an example code. If you have questions regarding this procedure, please contact your local Chips and Technologies, Inc. sales office.

B 2.0 Operation

In Standby mode, the 65550 suspends all CPU, memory, and display activities. It places the DRAM(s) in slow- or self-refresh mode (FR05[6]), and may shut off the 14.31818MHz reference clock and/or the 32KHz depending on the configuration of the chip during Standby.

In slow-refresh mode (FR05[6] = 1), using the internal RCLK (XRCF[3] = 0) for slow-refresh timing, the 14.31818MHz clock cannot be turned off. The 14.31818MHz clock generates the 37.5KHz RCLK used in the Standby slow-refresh timing. If the chip is using the external 32KHz on pin 154 (AA9) as the slow-refresh timing reference clock, then the 14.31818MHz clock can be shut off.

In self-refresh mode (FR05[6] = 0), the 14.31818MHz clock can be shut off. If the external 32KHz is also used, it can also be shut off during Standby.

The external 32KHz or internal RCLK is used for slow-refresh and panel power sequencing timing (XRCF[3]).

If the clock(s) may be shut off, they must be shut off after waiting twice the time programmed in FR04[3-0] (Panel Power Sequencing Delay Register - Power Down Delay) after the STNDBY# pin is asserted. This will allow the chip to completely finish all housekeeping activities after the STNDBY# pin is asserted.

When exiting Standby mode (Resume), the clocks must be applied (if turned off) to the chip and be stable before the STNDBY# pin may be de-asserted. After the STNDBY# pin has been de-asserted, the chip can be accessed after waiting twice the value time programmed in FR04[7-4] (Power Up Delay). This will allow the chip to fully come out of Standby.

The VGA subsystem dissipates a minimum amount of power during Standby. Since the 65550 is a fully static device, the contents of the controller's registers and on-chip palette are maintained during Standby. Therefore, Standby mode provides fast Suspend/Resume operations. Standby mode may be activated by asserting the STNDBY# pin low or programming FR05[4] = 1. The only way to come out of Standby is by de-asserting the STNDBY# pin.

The 65550 has been designed to minimize power consumption during Standby in either Panel-only or Simultaneous modes. During these modes, it is assumed that AC power is not available and the system is running on batteries. During CRT-only mode, it is assumed that AC power is available and therefore power consumption does not need to be minimized.

To minimize power consumption during CRT-only mode, then it is recommended that the chip switch to Panel only mode before entering Standby.

The 65550 has also been designed to enter Standby mode only from Normal operation mode, therefore the 65550 cannot enter Standby mode when in the Panel-Off mode (FR05[3] = 1). To enter Standby mode from Panel-Off mode, it is recommended that it first come out of Panel-Off mode (Panel-On mode - FR05[3] = 0) then enter Standby mode.

It must be remembered that after setting FR05[3] = 0 (Panel-On mode), the chip cannot enter Standby mode until waiting twice the value time programmed into FR04[7-4]. This will allow the chip to fully come out of Panel-Off mode.

The following example procedure and code assumes the chip is in Panel-only or Simultaneous modes and Normal operation before entering Standby.

B 3.0 Procedure

In order to provide optimal Suspend/Resume operation (Standby mode) with the 65550, the following software procedure must be implemented in either the system BIOS or the power management software.

1. Before Entering Suspend Mode

Software must execute the following procedure before asserting the STNDBY# pin of the 65550:

a) SAVE the contents of register 3C6h (Color Palette Pixel Mask Register).

b) PROGRAM register 3C6h to 00 - Disabling access to palette contents.

c) SAVE all DAC registers (Video DAC State and Color Registers) using the Video BIOS function call 5FA1h.

d) Enter Standby mode by asserting the STNDBY# pin of the 65550.

Wait a minimum time delay of twice the value programmed into register FR04[3-0] (Panel Power Sequencing Register - Power Down) in msec. before turning off the external 14.31818MHz oscillator (if applicable). This allows the 65550 to completely finish all activities ('housekeeping') after the STNDBY# pin is asserted .

2. After Exiting Suspend Mode (Resume)

The 14.31818MHz external oscillator must be applied to the 65550 and be stable before de-asserting the STNDBY# pin (if applicable). After de-asserting the STNDBY# pin of the 65550, the software must execute the following procedure:

a) Wait a minimum time delay of twice the value programmed into register FR04[7-4] (Power Up) in msec. This allows the 65550 to completely come out of Standby after the STNDBY# pin is de-asserted.

b) RESTORE all DAC registers (Video DAC State and Color Registers) using the Video BIOS function call 5FA2h.

c) RESTORE the saved contents of register 3C6h (Color Palette Pixel Mask Register).

The following pages show an example of the code.

Example Code

```
;-------------------------------------------------------------------------
; Module Name           : STANDBY.asm
; Program Name          : STANDBY.com
; Description           : Standby (550)
; Date                  : Sept 6, 1994
; Version               : 1.0
; Programmer            : Chips and Technologies, Inc.
; (C) 1995 Chips and Technologies, Inc.
;-------------------------------------------------------------------------
; Code Segment Starts
        code    segment
        assume  cs:code, ds:code, ss:code, es:code
        org     100h; for making program .COM type
begin:

STANDBY proc  near

;*************************************************************************************************
; This delay routine is incase the system is already in Standby.
;*************************************************************************************************
        mov     dx,3d0h                 ; Set to FR Index
        in      al,dx                   ; Read FR Index
        push    ax                      ; Save FR Index
        mov     al,04h                  ; Set Index to FR04
        out     dx,al
        in      ax,dx                   ; Read contents of FR04 (Panel Power Sequencing Delay
Register)
        mov     CS:FR04,ax              ; Save FR04
        pop     ax
        out     dx,al                   ; Restore FR Index
        call    Wdelay                  ; delay
```

```
;PREPARE FOR STANDBY
        mov     dx,3c6h
        in      al,dx                   ; Read Color Palette Pixel Mask Register
        mov     CS:D_3c6,al             ; Save Color Palette Pixel Mask Register
        mov     al,0
        out     dx,al                   ; Disable access to Palette contents
        mov     ax,5fa1h                ; Video BIOS function call to Save Video State
        mov     cx,04h                  ; Video DAC state
        push    cs
        pop     es
        mov     bx,offset Buff_DAC      ; Set Correct buffer
        int     10h                     ; Save

; [ A ] STANDBY
;*************************************************************************************
; Code to enter Standby should be placed here.  This code depends on the Standby
; implementation in the System
;*************************************************************************************
        call    Sdelay                  ; delay
;*************************************************************************************

; [ B] WAKE UP
;*************************************************************************************
;
; Code to exit Standby should be placed here.  This code depends on the Standby
; implementation in the System.
;
;*************************************************************************************
        call    Wdelay                  ;delay
; RESTORE STATE AFTER WAKEUP
        mov     ax,5fa2h                ; Video BIOS function call to Restore Video State
        mov     cx,04h                  ; Video DAC state and Color Registers
        push    cs
        pop     es
        mov     bx,offset Buff_DAC      ; From buffer
        int     10h                     ; Restore
        mov     dx,3c6h                 ; Set to Color Palette Pixel Mask Register
        mov     al,CS:D_3c6
        out     dx,al                   ; Restore Color Palette Pixel Mask Register
        ret                             ; Terminate
```

```
STANDBY     endp

; Wake-up delay routine
Wdelay  Proc    near

        mov     ax,CS:FR04
        and     ah,0f0h                 ; Select Power Up Delay (bits 4 - 7)
        .386
        shr     ah,1                    ; 8 times
        .286
        xor     cx,cx
        mov     cl,ah                   ; CX = delay count in msec
        call    delay                   ; Call User System Specific Delay Routine
        ret

Wdelay  endp

; Standby delay routine
Sdelay  Proc    near
        mov     ax,CS:FR04
        and     ah,0fh                  ; Select Power Down Delay (bits 3 - 0)
        mov     al,ah
        mov     ah,2*29                 ; msec
        mul     ah
        mov     cx,ax                   ; CX = delay count in msec
        call    delay                   ; Call User Specific Delay Routine
        ret

Sdelay  endp

; [C] User Specific Delay Routine
;*********************************************************************************************
; Code to implement User Specific Delay Routine goes here.
; This is to allow User to implement the delay routine based on the system requirements.
;
; Entry: CX = delay count in msec
;*********************************************************************************************
delay   Proc    near                    ; Delay

        ret
delay   endp
;*********************************************************************************************
```

```
;--------------------------
; Data Declaration
;--------------------------
D_3c6           db      ?
FR Index        db      ?
FR04            dw      ?
Buff_DAC        db      1000h dup(0)
code    ends
        end     begin
```

Note : [A], [B], and [C] should be implemented based on system requirements.

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