KSZ9031RNX

Gigabit Ethernet Transceiver with RGMII Support

Preliminary Data Sheet Rev 0.10

General Description

The KSZ9031RNX is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9031RNX provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000 Mbps speed.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

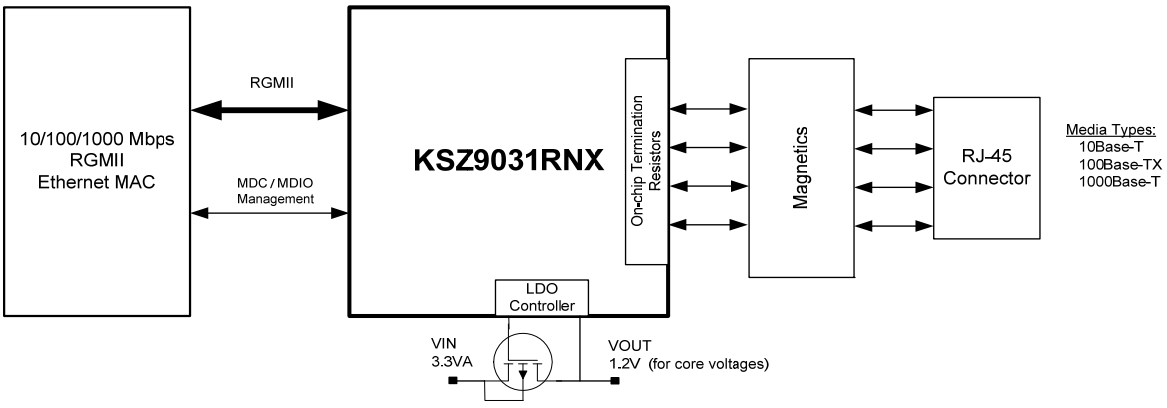
The KSZ9031RNX provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9031 I/Os and board. Remote and local loopback functions provide verification of analog and digital data paths.

The KSZ9031RNX is available in the 48-pin lead-free QFN package (See Ordering Information).

Features

- Single-chip 10/100/1000 Mbps IEEE 802.3 compliant Ethernet Transceiver
- RGMII timing supports internal delay with programming options for external delay and to make adjustment and correction to Tx and Rx timing paths
- RGMII I/Os with 3.3V/2.5V/1.8V tolerant
- Auto-Negotiation to automatically select the highest link up speed (10/100/1000 Mbps) and duplex (half/full)
- On-chip termination resistors for the differential pairs
- On-chip LDO controller to support single 3.3V supply operation – requires only external FET to generate 1.2V for the core
- Jumbo frame support up to 16KB
- 125 MHz Reference Clock Output
- Programmable LED outputs for link, activity and speed
- Baseline Wander Correction
- Energy Detect Power Down Mode for reduced power consumption when cable not attached
- Energy Efficient Ethernet (EEE) support
- Wake On LAN (WOL) Support with robust custom packet detection

Functional Diagram



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More Features

- Parametric NAND Tree support for fault detection between chip I/Os and board.
- Loopback modes for diagnostics
- Automatic MDI/MDI-X crossover for detection and correction of pair swap at all speeds of operation
- Automatic detection and correction of pair swap, pair skew and pair polarity
- MDC/MDIO Management Interface for PHY register configuration
- Interrupt pin option
- Power down and power saving modes
- Operating Voltages
  - Core: 1.2V (external FET or regulator)
  - I/O: 1.8V, 2.5V, or 3.3V
  - Transceiver: 3.3V
- Available package
  - 48-pin QFN (7mm x 7mm)

Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Gigabit LAN on Motherboard (GLOM)
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-top Box
- Game Console
- Triple-play (data, voice, video) Media Center
- Media Converter

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Wire Bonding	Description
KSZ9031RNXCA	0°C to 70°C	48-Pin QFN	Pb-Free	Gold	RGMII, Commercial Temperature, Gold Wire Bonding
KSZ9031RNXIA (1)	–40°C to 85°C	48-Pin QFN	Pb-Free	Gold	RGMII, Industrial Temperature, Gold Wire Bonding
KSZ9031RNX-EVAL	0°C to 70°C	48-Pin QFN	Pb-Free		KSZ9031RNX Evaluation Board (Mounted with KSZ9031RNX device in commercial temperature)

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
0.1	8/10/10	Preliminary Data sheet created.
0.2	10/29/10	Change core voltage to 1.2V. Added note for Energy Efficient Ethernet (EEE) Registers to be added. Changed PHY Identifiers for register 2h and 3h to TBD (will be added when values are assigned). Removed Extended Registers (to be revised and added in a later revision). Added 2.5V VDD I/O parameters to Electrical Table. Added LED drive current. Updated boilerplate.
0.3	06/09/11	Updated pin out picture, updated some in pin descriptions
0.4	06/13/11	Misc edits Put in register info from 9031GN Rev 0.7, 6/09/11 Updated strapping options section
0.5	07/07/11	Put in register info from 9031GN Rev 0.11, 7/05/11 and latest engineering inputs Took out references to LinkMD Added EDPD mode info and associated register information Updated RGMII info in registers
0.6	07/07/11	Updated the EEE feature area with new timing diagrams for RMII method.
0.7	07/08/11	Cleaned up some register information, strapping info, and misc items.
0.8	11/15/11	Added current / power consumption section.
0.9	11/16/11	Updated current / power consumption section.
0.10	5/23/12	Re-formatted and cleaned up data sheet. Corrected ISET resistor value. Added power-up requirements. Updated Reference Circuits – LED Strap-in Pins section. Changed part number from KSZ9031RN to KSZ9031RNX throughout data sheet. Updated Ordering Information. Updated current / power consumption values.

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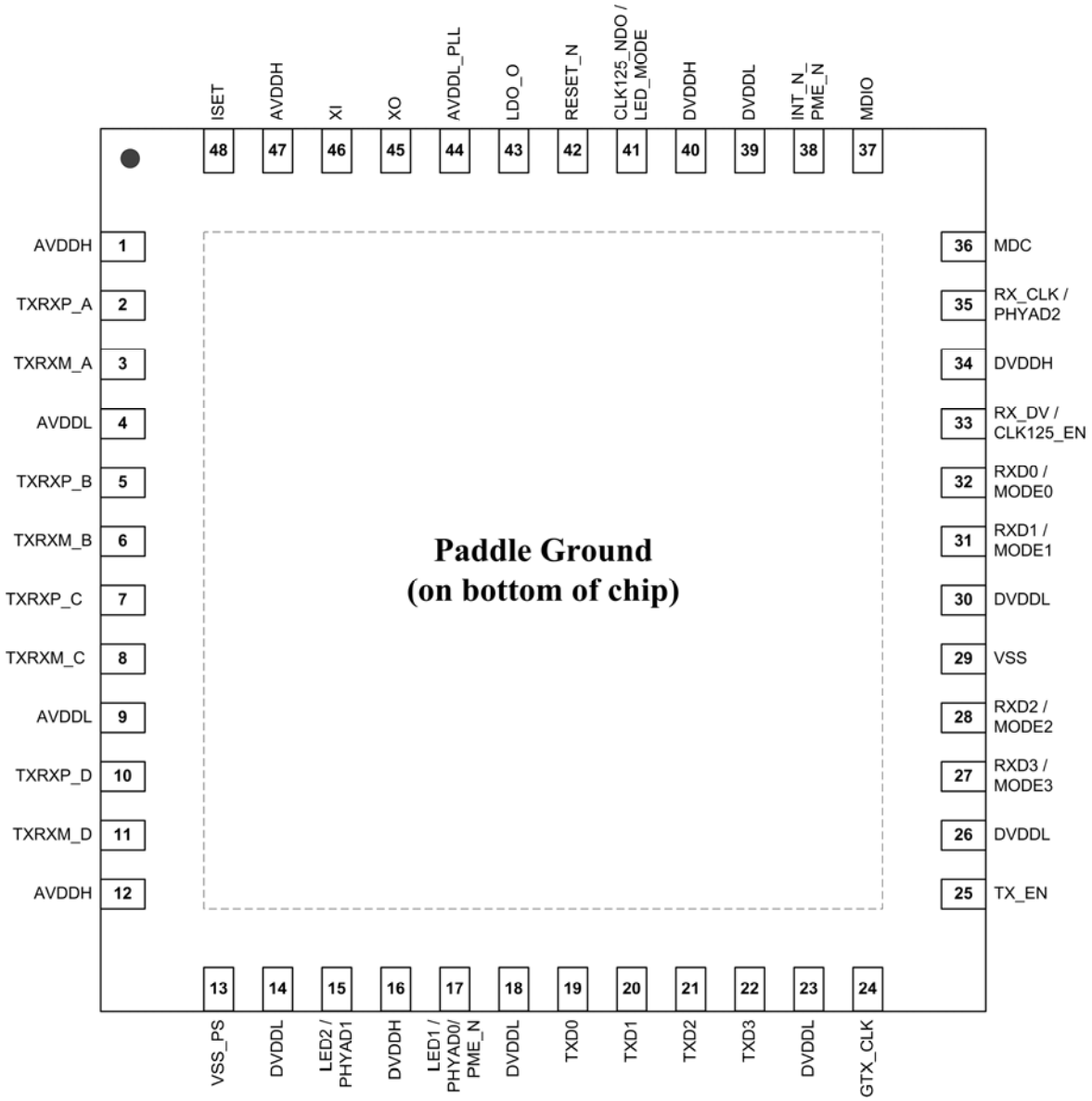


48-Pin QFN
(Top View)

Pin Description – KSZ9031RNX

Pin Number	Pin Name	Type[1]	Pin Function
1	AVDDH	P	3.3V analog V_{DD}
2	TXRXP_A	I/O	Media Dependent Interface[0], positive signal of differential pair 1000Base-T Mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
3	TXRXM_A	I/O	Media Dependent Interface[0], negative signal of differential pair 1000Base-T Mode: TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively.
4	AVDDL	P	1.2V analog V_{DD}
5	TXRXP_B	I/O	Media Dependent Interface[1], positive signal of differential pair 1000Base-T Mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
6	TXRXM_B	I/O	Media Dependent Interface[1], negative signal of differential pair 1000Base-T Mode: TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively.
7	TXRXP_C	I/O	Media Dependent Interface[2], positive signal of differential pair 1000Base-T Mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_C is not used.
8	TXRXM_C	I/O	Media Dependent Interface[2], negative signal of differential pair 1000Base-T Mode: TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_C is not used.
9	AVDDL	P	1.2V analog V_{DD}

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>10</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair
1000Base-T Mode:
TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.
10Base-T / 100Base-TX Mode:
TXRXP_D is not used.</td></tr>
<tr><td>11</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair
1000Base-T Mode:
TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively.
10Base-T / 100Base-TX Mode:
TXRXM_D is not used.</td></tr>
<tr><td>12</td><td>AVDDH</td><td>P</td><td>3.3V analog V_{DD}</td></tr>
<tr><td>13</td><td>VSS_PS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>14</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>15</td><td>LED2 /
PHYAD1</td><td>I/O</td><td>LED Output: Programmable LED2 Output
Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up / reset. See “Strapping Options” section for details.
The LED2 pin is programmed by the LED_MODE strapping option (pin 41), and is defined as follows.

Single LED Mode
<table><tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>Link off</td><td>H</td><td>OFF</td></tr><tr><td>Link on (any speed)</td><td>L</td><td>ON</td></tr></table>
Tri-color Dual LED Mode
<table><tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr><tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr><tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr><tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr><tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr><tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr><tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr><tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr><tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr></table>
For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 17) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>16</td><td>DVDDH</td><td>P</td><td>3.3V / 2.5V / 1.8V digital V_{DD}</td></tr>
</table>

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>17</td><td>LED1 /
PHYAD0 /
PME_N</td><td>I/O</td><td>LED1 Output: Programmable LED1 Output
Config Mode: The voltage on this pin is sampled and latched during the power-up / reset process to determine the value of PHYAD[0]. See the “Strapping Options” section for details.
PME_N: WOL Event indicator. When low, one of three possible WOL events has occurred.

Single LED Mode
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table>
Tri-color Dual LED Mode
<table>
<tr><th rowspan="2">Link / Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 15) to indicate 10 Mbps Link and Activity.</td></tr>
<tr><td>18</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>19</td><td>TXD0</td><td>I</td><td>RGMII Mode: RGMII TD0 (Transmit Data 0) Input</td></tr>
<tr><td>20</td><td>TXD1</td><td>I</td><td>RGMII Mode: RGMII TD1 (Transmit Data 1) Input</td></tr>
<tr><td>21</td><td>TXD2</td><td>I</td><td>RGMII Mode: RGMII TD2 (Transmit Data 2) Input</td></tr>
<tr><td>22</td><td>TXD3</td><td>I</td><td>RGMII Mode: RGMII TD3 (Transmit Data 3) Input</td></tr>
<tr><td>23</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>24</td><td>GTX_CLK</td><td>I</td><td>RGMII Mode: RGMII TXC (Transmit Reference Clock) Input</td></tr>
<tr><td>25</td><td>TX_EN</td><td>I</td><td>RGMII Mode: RGMII TX_CTL (Transmit Control) Input</td></tr>
<tr><td>26</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>27</td><td>RXD3 /
MODE3</td><td>I/O</td><td>RGMII Mode: RGMII RD3 (Receive Data 3) Output /
Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up / reset. See “Strapping Options” section for details.</td></tr>
<tr><td>28</td><td>RXD2 /
MODE2</td><td>I/O</td><td>RGMII Mode: RGMII RD2 (Receive Data 2) Output /
Config Mode: The pull-up/pull-down value is latched as MODE2 during power-up / reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>VSS</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>30</td><td>DVDDL</td><td>P</td><td>1.2V digital V_{DD}</td></tr>
<tr><td>31</td><td>RXD1 /
MODE1</td><td>I/O</td><td>RGMII Mode: RGMII RD1 (Receive Data 1) Output /
Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up / reset. See “Strapping Options” section for details.</td></tr>
</table>

Pin Number	Pin Name	Type(1)	Pin Function
32	RXD0 / MODE0	I/O	RGMII Mode: RGMII RD0 (Receive Data 0) Output / Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up / reset. See “Strapping Options” section for details.
33	RX_DV / CLK125_EN	I/O	RGMII Mode: RGMII RX_CTL (Receive Control) Output / Config Mode: Latched as CLK125_NDO Output Enable during power-up / reset. See “Strapping Options” section for details.
34	DVDDH	P	3.3V / 2.5V / 1.8V digital V_{DD}
35	RX_CLK / PHYAD2	I/O	RGMII Mode: RGMII RXC (Receive Reference Clock) Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up / reset. See “Strapping Options” section for details.
36	MDC	Ipu	Management Data Clock Input This pin is the input reference clock for MDIO (pin 37).
37	MDIO	Ipu/O	Management Data Input / Output This pin is synchronous to MDC (pin 36) and requires an external pull-up resistor to 3.3V digital V_{DD} in a range from 1.0KΩ to 4.7KΩ.
38	INT_N / PME_N	O	Interrupt Output This pin provides a programmable interrupt output and requires an external pull-up resistor to 3.3V digital V_{DD} in a range from 1.0KΩ to 4.7KΩ when active low. Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 14 sets the interrupt output to active low (default) or active high.
39	DVDDL	P	1.2V digital V_{DD}
40	DVDDH	P	3.3V / 2.5V / 1.8V digital V_{DD}
41	CLK125_NDO / LED_MODE	I/O	125 MHz Clock Output This pin provides a 125 MHz reference clock output option for use by the MAC. / Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up / reset. See “Strapping Options” section for details.
42	RESET_N	Ipu	Chip Reset (active low) Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See “Strapping Options” section for more details.
43	LDO_O	O	On-chip 1.2V LDO Controller Output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip’s core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating.
44	AVDDL_PLL	P	1.2V analog V_{DD} for PLL
45	XO	O	25 MHz Crystal feedback This pin is a no connect if oscillator or external clock source is used.
46	XI	I	Crystal / Oscillator / External Clock Input 25 MHz +/-50ppm tolerance
47	AVDDH	P	3.3V analog V_{DD}
48	ISET	I/O	Set transmit output level Connect a 12.1KΩ 1% resistor to ground on this pin.
PADDLE	P_GND	Gnd	Exposed Paddle on bottom of chip Connect P_GND to ground.

Note:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up.
   Ipu/O = Input with internal pull-up / Output.

Strapping Options – KSZ9031RNX

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>35

15

17</td><td>RXCLK/
PHYAD2

LED2/
PHYAD1

LED1/
PHYAD0/
PME_N</td><td>I/O

I/O

I/O</td><td>The PHY Address, PHYAD[2:0], is sampled and latched at power-up / reset and is configurable to any value from 1 to 7. Each PHY address bit is configured as follows:
Pull-up = 1
Pull-down = 0
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>27

28

31

32</td><td>RXD3/
MODE3

RXD2/
MODE2

RXD1/
MODE1

RXD0/
MODE0</td><td>I/O

I/O

I/O

I/O</td><td>The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table>
<tr><th>MODE[3:0]</th><th>Mode</th></tr>
<tr><td>0000</td><td>RGMII Mode</td></tr>
<tr><td>0001</td><td>Reserved – not used</td></tr>
<tr><td>0010</td><td>Reserved – not used</td></tr>
<tr><td>0011</td><td>Reserved – not used</td></tr>
<tr><td>0100</td><td>NAND Tree Mode</td></tr>
<tr><td>0101</td><td>Reserved – not used</td></tr>
<tr><td>0110</td><td>Reserved – not used</td></tr>
<tr><td>0111</td><td>Chip Power Down Mode</td></tr>
<tr><td>1000</td><td>RGMII Mode & PME_N on LED1 Pin</td></tr>
<tr><td>1001</td><td>Reserved – not used</td></tr>
<tr><td>1010</td><td>RGMII Mode & PME_N on INT_N Pin</td></tr>
<tr><td>1011</td><td>Reserved – not used</td></tr>
<tr><td>1100</td><td>RGMII Mode – advertise 1000Base-T full-duplex only</td></tr>
<tr><td>1101</td><td>RGMII Mode – advertise 1000Base-T full and half-duplex only</td></tr>
<tr><td>1110</td><td>RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex),except 1000Base-T half-duplex</td></tr>
<tr><td>1111</td><td>RGMII Mode – advertise all capabilities (10/100/1000 speed half/full duplex)</td></tr>
</table></td></tr>
<tr><td>33</td><td>CLK125_EN</td><td>I/O</td><td>CLK125_EN is latched at power-up / reset and is defined as follows:
Pull-up = Enable 125 MHz Clock Output
Pull-down = Disable 125 MHz Clock Output
Pin 41 (CLK125_NDO) provides the 125 MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>41</td><td>LED_MODE</td><td>I/O</td><td>LED_MODE is latched at power-up / reset and is defined as follows:
Pull-up = Single LED Mode
Pull-down = Tri-color Dual LED Mode</td></tr>
</table>

Note:

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

Functional Overview

The KSZ9031RNX is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable. Its on-chip proprietary 1000Base-T transceiver and Manchester/MLT-3 signaling-based 10Base-T/100Base-TX transceivers are all IEEE 802.3 compliant.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9031RNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9031RNX provides the RGMII interface for a direct and seamless connection to RGMII MACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000 Mbps speed.

The following figure shows a high-level block diagram of the KSZ9031RNX.

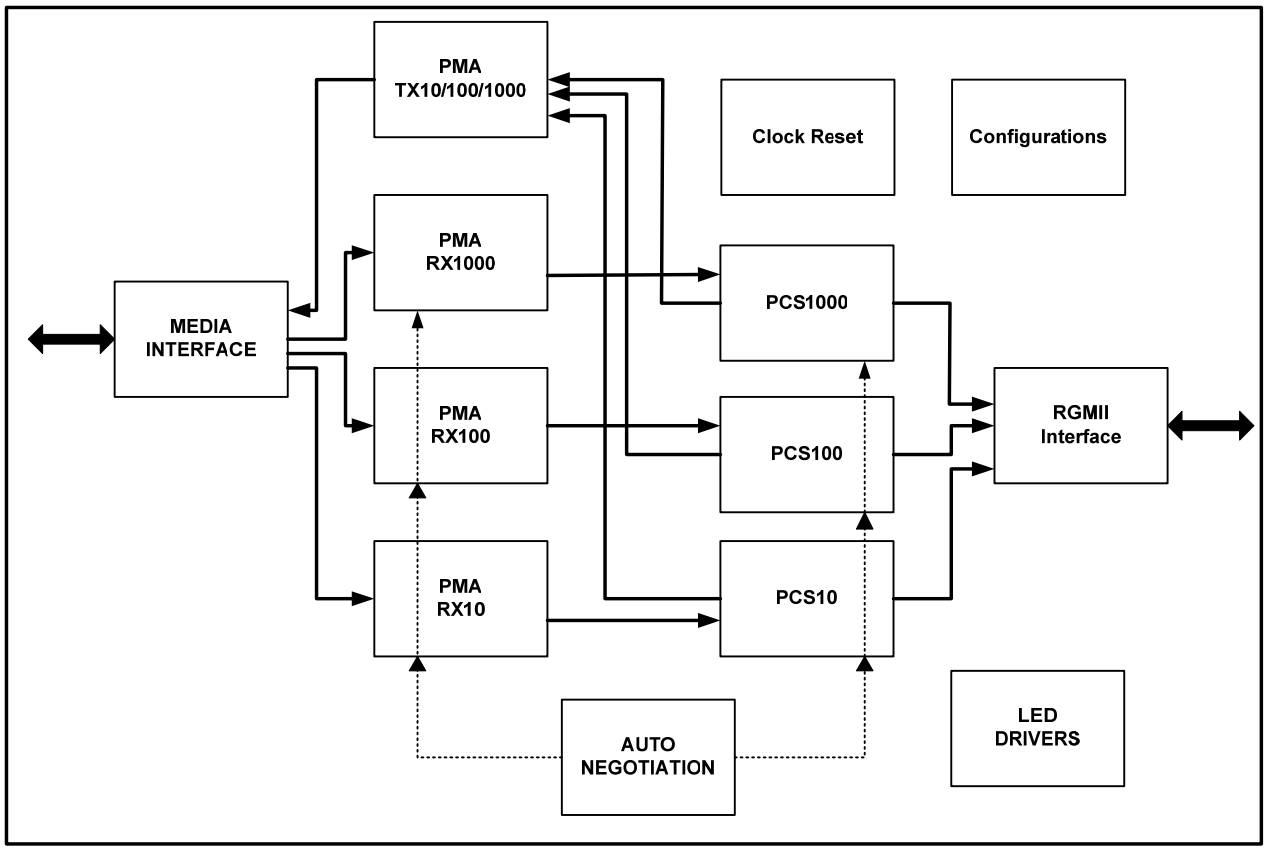


Figure 1. KSZ9031RNX Block Diagram

Functional Description: 10Base-T/100Base-TX Transceiver

100Base-TX Transmit

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the RGMII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 12.1KΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10Base-T Transmit

The output 10Base-T driver is incorporated into the 100Base-TX driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into typical outputs of 2.5V amplitude. The harmonic contents are at least 31 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9031RNX decodes a data frame. The receiver clock is maintained active during idle periods in between receiving data frames.

Functional Description: 1000Base-T Transceiver

The 1000Base-T transceiver is based on a mixed-signal/digital signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancellers, cross-talk cancellers, precision clock recovery scheme, and power efficient line drivers.

The following figure shows a high-level block diagram of a single channel of the 1000Base-T transceiver for one of the four differential pairs.

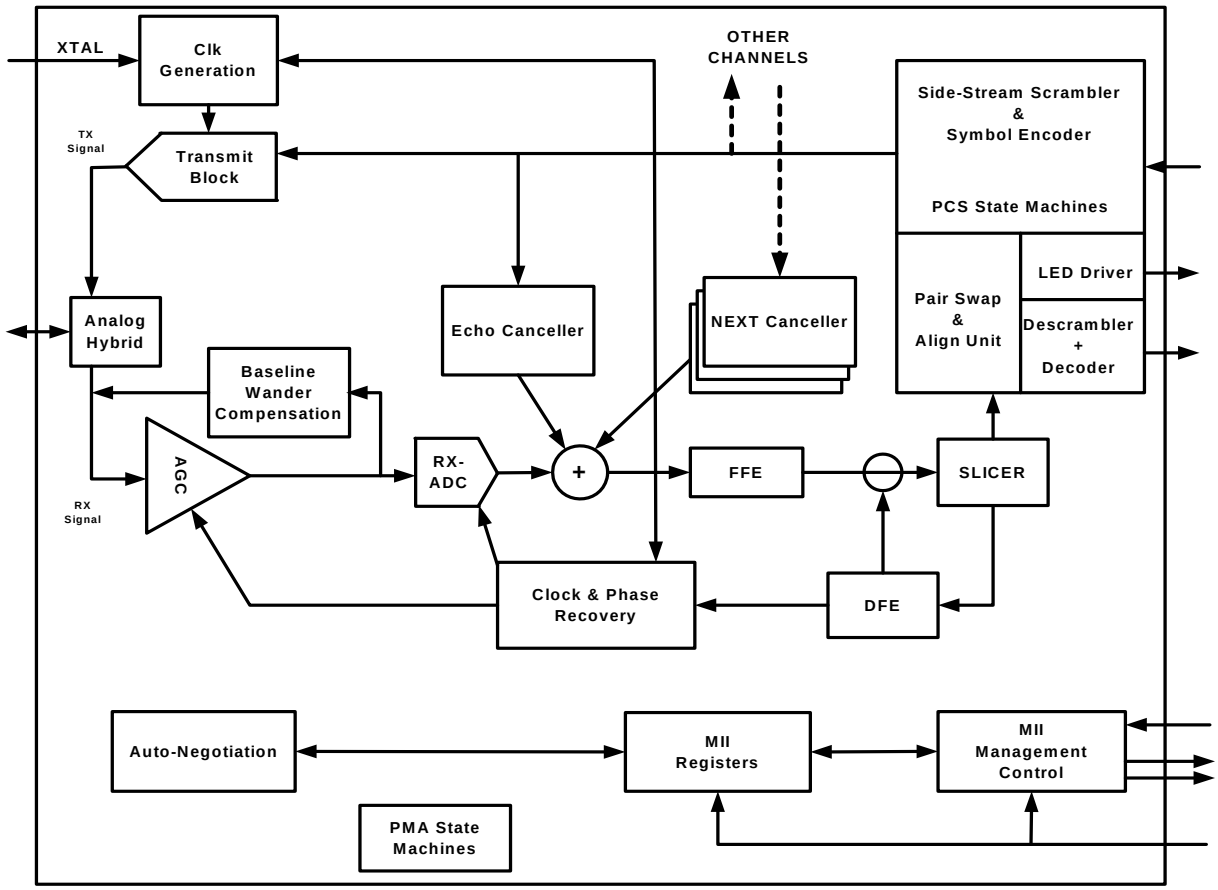


Figure 2. KSZ9031RNX 1000Base-T Block Diagram – Single Channel

Analog Echo Cancellation Circuit

In 1000Base-T mode, the analog echo cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10Base-T/100Base-TX mode.

Automatic Gain Control (AGC)

In 1000Base-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

Analog-to-Digital Converter (ADC)

In 1000Base-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10Base-T/100Base-TX mode.

Timing Recovery Circuit

In 1000Base-T mode, the mixed-signal clock recovery circuit, together with the digital phase locked loop, is used to recover and track the incoming timing information from the received data. The digital phase locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000Base-T slave PHY is required to transmit the exact receive clock frequency recovered from the received data back to the 1000Base-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. Additionally, this helps to facilitate echo cancellation and NEXT removal.

Adaptive Equalizer

In 1000Base-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid and echo due to impedance mismatch. The KSZ9031RNX employs a digital echo canceller to further reduce echo components on the receive signal.

In 1000Base-T mode, the data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high frequency cross-talk coming from adjacent wires. The KSZ9031RNX employs three NEXT cancellers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10Base-T/100Base-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

Trellis Encoder and Decoder

In 1000Base-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9031RNX is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order and polarity have to be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and then de-scrambled into 8-bit data.

Functional Description: 10/100/1000 Transceiver Features

Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9031RNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and then assigns the MDI/MDI-X pair mapping of the KSZ9031RNX accordingly.

The following table shows the KSZ9031RNX 10/100/1000 pin-out assignments for MDI/MDI-X pin mapping.

Pin (RJ-45 pair)	MDI			MDI-X		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
TXRXP/M_A (1,2)	A+/-	TX+/-	TX+/-	B+/-	RX+/-	RX+/-
TXRXP/M_B (3,6)	B+/-	RX+/-	RX+/-	A+/-	TX+/-	TX+/-
TXRXP/M_C (4,5)	C+/-	Not used	Not used	D+/-	Not used	Not used
TXRXP/M_D (7,8)	D+/-	Not used	Not used	C+/-	Not used	Not used

Table 1. MDI / MDI-X Pin Mapping

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to Reg. 28 (1Ch) bit 6. MDI and MDI-X mode is set by Reg. 28 (1Ch) bit 7 if auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

Pair- Swap, Alignment, and Polarity Check

In 1000Base-T mode, the KSZ9031RNX

- Detects incorrect channel order and automatically restore the pair order for the A, B, C, D pairs (four channels)
- Supports 50±10ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected 4-pairs of data symbols are synchronized

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

Wave Shaping, Slew Rate Control and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000Base-T, a special partial response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100Base-TX, a simple slew rate control method is used to minimize EMI.
- For 10Base-T, pre-emphasis is used to extend the signal quality through the cable.

PLL Clock Synthesizer

The KSZ9031RNX generates 125 MHz, 25 MHz and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

Auto-Negotiation

The KSZ9031RNX conforms to the Auto-Negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-Negotiation allows UTP (Unshielded Twisted Pair) link partners to select the highest common mode of operation.

During Auto-Negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 1000Base-T, full-duplex
- Priority 2: 1000Base-T, half-duplex
- Priority 3: 100Base-TX, full-duplex
- Priority 4: 100Base-TX, half-duplex
- Priority 5: 10Base-T, full-duplex
- Priority 6: 10Base-T, half-duplex

If Auto-Negotiation is not supported or the KSZ9031RNX link partner is forced to bypass Auto-Negotiation for 10Base-T and 100Base-TX modes, then the KSZ9031RNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9031RNX to establish a link by listening for a fixed signal protocol in the absence of Auto-Negotiation advertisement protocol.

The Auto-Negotiation link up process is shown in the following flow chart.

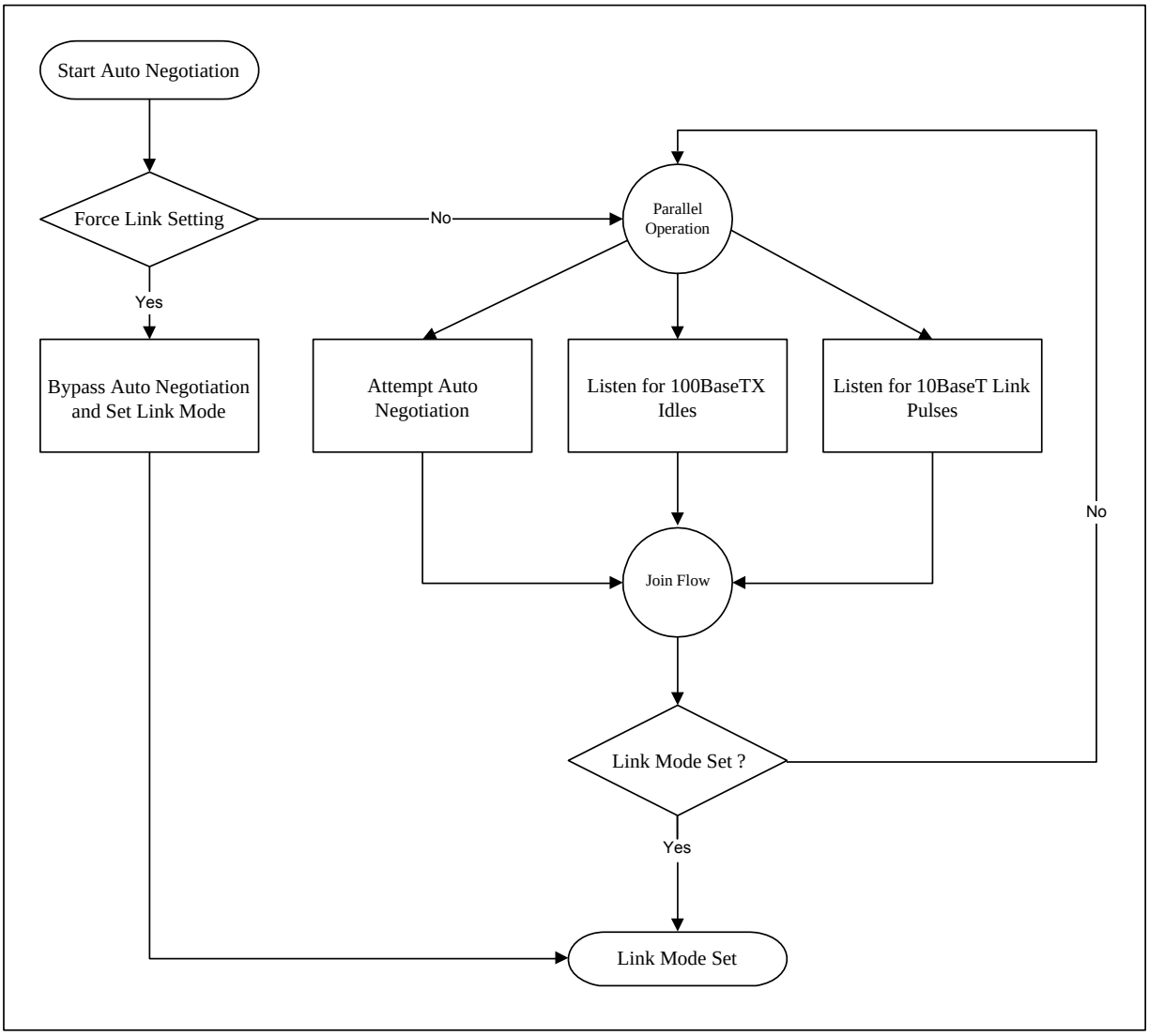


Figure 3. Auto-Negotiation Flow Chart

For 1000Base-T mode, Auto-Negotiation is required and always used to establish link. During 1000Base-T Auto-Negotiation, Master and Slave configuration is first resolved between link partners, and then link is established with the highest common capabilities between link partners.

Auto-Negotiation is enabled by default at power-up or after hardware reset. Afterwards, Auto-Negotiation can be enabled or disabled through Reg. 0h bit 12. If Auto-Negotiation is disabled, then the speed is set by Reg. 0h bits 6 and 13, and the duplex is set by Reg. 0h bit 8.

If the speed is changed on the fly, then the link goes down and either Auto-Negotiation or parallel detection will initiate until a common speed between KSZ9031RNX and its link partner is re-established for link.

If link is already established, and there is no change of speed on the fly, then the changes will not take effect unless either Auto-Negotiation is restarted through Reg. 0h bit 9, or a link down to link up transition occurs (i.e., disconnecting and reconnecting the cable).

After Auto-Negotiation is completed, the link status is updated in register 1 and the link partner capabilities are updated in Reg. 05h, 06h, and 0Fh.

The Auto-Negotiation finite state machines employ interval timers to manage the Auto-Negotiation process. The duration of these timers under normal operating conditions are summarized in the following table.

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst interval	16 ms
Transmit Pulse interval	68 us
FLP detect minimum time	17.2 us
FLP detect maximum time	185 us
Receive minimum Burst interval	6.8 ms
Receive maximum Burst interval	112 ms
Data detect minimum interval	35.4 us
Data detect maximum interval	95 us
NLP test minimum interval	4.5 ms
NLP test maximum interval	30 ms
Link Loss time	52 ms
Break Link time	1480 ms
Parallel Detection wait time	830 ms
Link Enable wait time	1000 ms

Table 2. Auto-Negotiation Timers

RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) is compliant with the RGMII Version 1.3 Specification. It provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10 Mbps, 100 Mbps, and 1000 Mbps) are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

In RGMII operation, the RGMII pins function as follow:

- The MAC sources the transmit reference clock, TXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, RXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- For 1000Base-T, the transmit data, TXD[3:0], is presented on both edges of TXC, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125 MHz clock, RXC.
- For 10Base-T/100Base-TX, the MAC will hold TX_CTL low until both PHY and MAC operate at the same speed. During the speed transition, the receive clock will be stretched on either positive or negative pulse to ensure that no clock glitch is presented to the MAC at any time.
- TX_ER and RX_ER are combined with TX_EN and RX_DV, respectively, to form TX_CTL and RX_CTL. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the KSZ9031RNX is configured to RGMII mode if the MODE[3:0] strap-in pins are set to one of the RGMII mode capability options. See Strapping Options section for available options.

The KSZ9031RNX has the option to output a low jitter 125 MHz reference clock on the CLK125_NDO pin. This clock provides a lower cost reference clock alternative for RGMII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

RGMII Signal Definition

The following table describes the RGMII signals. Refer to the RGMII Version 1.3 Specification for more detailed information.

RGMII Signal Name (per spec)	RGMII Signal Name (per KSZ9031RNX)	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TXC	GTX_CLK	Input	Output	Transmit Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
TX_CTL	TX_EN	Input	Output	Transmit Control
TXD[3:0]	TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	RX_CLK	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_CTL	RX_DV	Output	Input	Receive Control
RXD[3:0]	RXD[3:0]	Output	Input	Receive Data [3:0]

Table 3. RGMII Signal Definition

RGMII Signal Diagram

The KSZ9031RNX RGMII pin connections to the MAC are shown in the following figure.

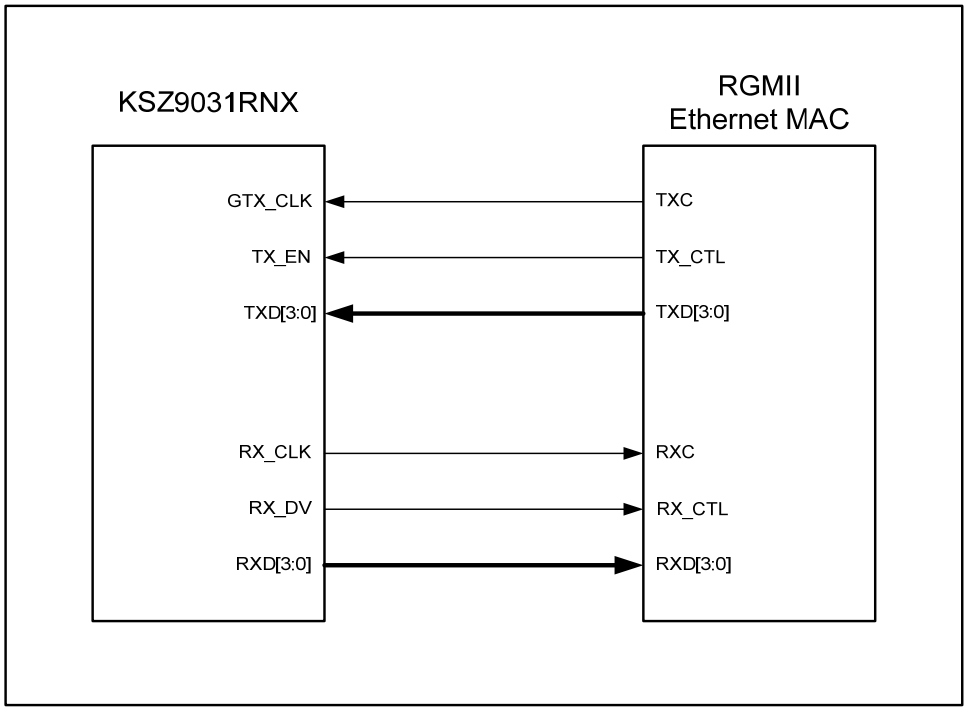


Figure 4. KSZ9031RNX RGMII Interface

RGMII In-band Status

The KSZ9031RNX can provide in-band status to the MAC during the inter-frame gap when RX_DV is de-asserted. RGMII in-band status is disabled by default. It is enabled by writing a one to extended Reg. 256 (100h) bit 8.

The in-band status is sent to the MAC using the RXD[3:0] data pins, and is described in the following table.

RX_DV	RXD3	RXD[2:1]	RXD0
0 (valid only when RX_DV is low and Reg. 256 (100h) bit 8 is set to 1)	Duplex Status 0 = half-duplex 1 = full-duplex	RX_CLK clock speed 00 =2.5 MHz 01 =25 MHz 10 =125 MHz 11 = reserved	Link Status 0 = Link down 1 = Link up

Table 4. RGMII In-Band Status

MII Management (MIIM) Interface

The KSZ9031RNX supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9031RNX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further detail on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with one or more KSZ9031RNX device. Each KSZ9031RNX device is assigned a PHY address between 1 and 7 by the PHYAD[2:0] strapping pins.
- A 32 register address space to access the KSZ9031RNX IEEE Defined Registers, Vendor Specific Registers and Extended Registers. See Register Map section.

The following table shows the MII Management frame format for the KSZ9031RNX.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 5. MII Management Frame Format – for KSZ9031RNX

Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9031RNX PHY register. Bits [15:8] of Reg. 27 (1Bh) are the interrupt control bits to enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of register 27 (1Bh) are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Reg. 27 (1Bh).

Bit 14 of Reg. 31 (1Fh) sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9031RNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

LED Mode

The KSZ9031RNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in pin. It is latched at power-up/reset and is defined as follows:

- Pull-up: Single LED Mode
- Pull-down: Tri-color Dual LED Mode

Single LED Mode

In Single LED Mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in the following table.

LED pin	Pin State	LED Definition	Link / Activity
LED2	H	OFF	Link off
	L	ON	Link on (any speed)
LED1	H	OFF	No Activity
	Toggle	Blinking	Activity (RX, TX)

Table 6. Single LED Mode – Pin Definition

Tri-color Dual LED Mode

In Tri-color Dual LED Mode, the Link and Activity status are indicated by the LED2 pin for 1000Base-T, by the LED1 pin for 100Base-TX, and by both LED2 and LED1 pin, working in conjunction, for 10Base-T. This is summarized in the following table.

LED Pin (State)		LED Pin (Definition)		Link / Activity
LED2	**LED1**	**LED2**	**LED1**	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link / No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

Table 7. Tri-color Dual LED Mode – Pin Definition

Each LED output pin can directly drive a LED with a series resistor (typically 220Ω to 470Ω).

For activity indication, the LED output toggles at approximately 12.5Hz (80ms) to ensure visibility to the human eye.

NAND Tree Support

The KSZ9031RNX provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to “0100”.

The following tables list the NAND tree pin order for KSZ9031RNX.

Pin	Description
LED2	Input
LED1	Input
TXD0	Input
TXD1	Input
TXD2	Input
TXD3	Input
GTX_CLK	Input
TX_EN	Input
RX_DV	Input
RX_CLK	Input
INT_N	Input
MDC	Input
MDIO	Input
CLK125_NDO	Output

Table 8. NAND Tree Test Pin Order – for KSZ9031RNX

Power Management

The KSZ9031RNX offers the following power management modes:

Power Saving Mode

This mode is a KSZ9031RNX green feature to reduce power consumption when the cable is unplugged. It is in effect when Auto-Negotiation mode is enabled and the cable is disconnected (no link).

Software Power Down Mode

This mode is used to power down the KSZ9031RNX device when it is not in use after power-up. S/W Power-Down Mode is enabled by writing a one to Reg. 0h bit 11. In the S/W Power-Down state, the KSZ9031RNX disables all internal functions, except for the MII management interface. The KSZ9031RNX exits S/W Power-Down mode after writing a zero to Reg. 0h bit 11.

Chip Power Down Mode

This mode provides the lowest power state for the KSZ9031RNX when it is not in use and is mounted on the board. Chip Power-Down Mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to “0111”. The KSZ9031RNX exits chip power down mode when a hardware reset is applied to the RESET_N pin with the MODE[3:0] strap-in pins set to an operating mode other than Chip Power-Down Mode.

Energy Detect Power Down Mode

Energy Detect Power Down Mode is used to further reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a “1” to the EDPD_EN bit, [MMD Device ID = 28h, Reg. 23h, bit 0] and is in effect when Auto-Negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ9031RNX shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Additional power consumption is achieved by extending the time interval in between transmission of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure two link partners in the same low power state and with Auto-MDI/MDI-X disabled can wake up when the cable is connected between them. By default, Energy Detect Power Down Mode is disabled after power-up.

Energy Efficient Ethernet (EEE)

The KSZ9031RNX implements Energy Efficient Ethernet (EEE) as described in IEEE 802.3AZ (Rev. 3.2). The standard is defined around a MAC that supports special signaling associated with EEE. EEE saves power by keeping the voltage on the Ethernet cable at approximately 0V for as often as possible during periods of no traffic activity. This is called Low Power mode or state (LPI). However, the link will respond automatically when traffic resumes and do so in such a way as to not cause blocking or dropping of any packets. (The wake up time for 100BT is specified to be less then 30uS. The wake up time for 1000BT is specified to be less then 16uS.) The transmit and receive directions are independently controlled. Note the EEE is not specified or implemented for 10BT. In 10BT, the transmitter is already OFF during idle periods.

The time during which LPI mode is active is during what is called Quiet time. This is shown in Figure 5.

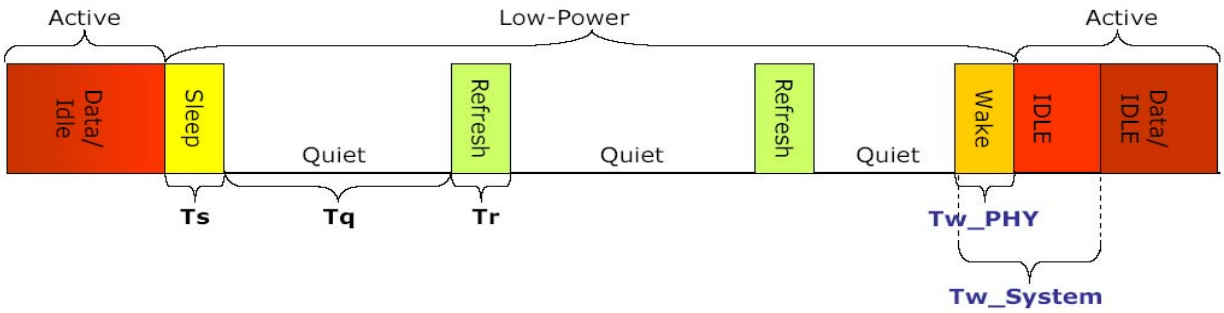


Figure 5 Traffic Activity and EEE

Transmit Direction Control

Low Power Idle (LPI) state for the transmit direction will be entered when the attached EEE MAC …TBD The KSZ9031RNX will stay in the Transmit LPI state while these signals remain in this state. For Gigabit Ethernet (1000BT), the TXC clock can be stopped by the MAC after the LPI signals have been asserted for 10 or more TXC cycles in order to save additional power. This timing is illustrated in Figure 6.

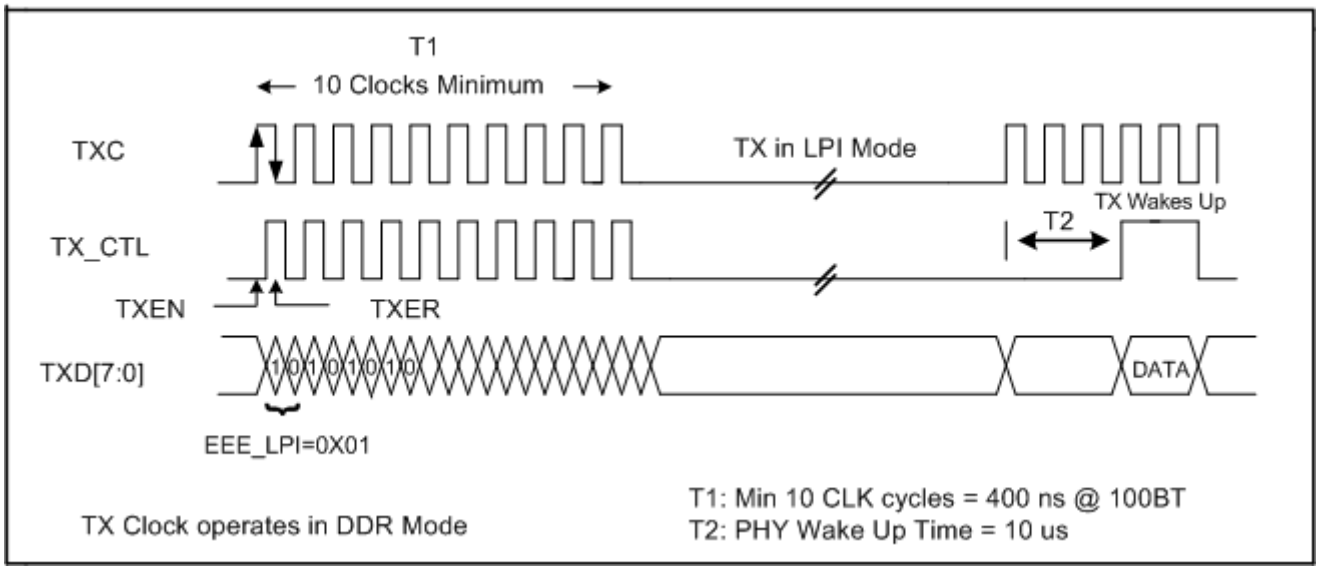


Figure 6 EEE Transmit Timing

Even though the PHY is in LPI state, it will periodically leave the LPI state to transmit a refresh signal using specific transmit code bits. This allows the link partner to keep track of the long term variation of channel characteristics and clock drift between the two partners. Approximately every 20-22 milliseconds, the PHY will transmit a bit pattern to its link partner of duration 200-220 microseconds. The Refresh times are shown in Figure 5.

Receive Direction Control

Exact description of this process is TBD. The KSZ9031RNX will stay in the Receive LPI state while these signals remain in this state. The PHY can turn off the RXC clock after 10 or more clocks have occurred in the LPI state. This is

accomplished by setting bit 11 in MDD Device ID = 3h / Reg. 0h. This timing is illustrated in Figure 7.

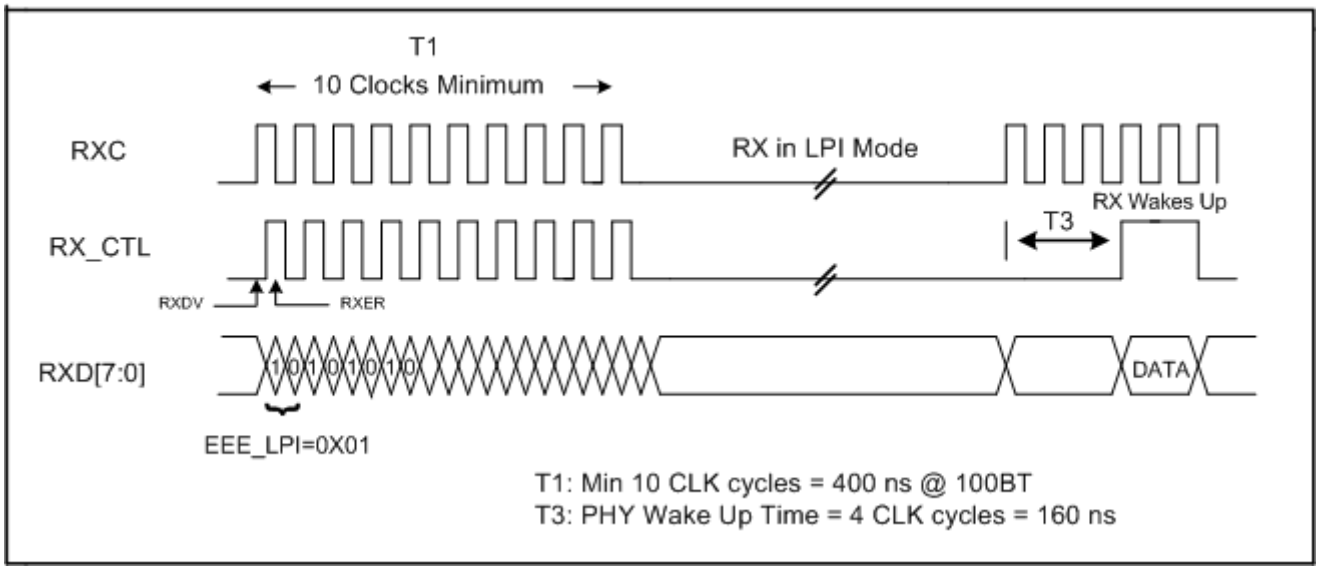


Figure 7 EEE Receive Timing

In the EEE compliant environment, the PHYs will be monitoring and expecting the P Code (Refresh) bit pattern from its link partner that is generated approximately every 20-22 milliseconds, with a duration of about 200-220 microseconds. This allows the link partner to keep track of the long term variation of channel characteristics and clock drift between the two partners.

Registers Associated with EEE

The following registers are used to configure or manage the EEE feature.

- Device ID = 03h, Reg. 01h - PCS EEE Status Register
- Device ID = 03h, Reg. 14h - EEE Cap Status Register
- Device ID = 03h, Reg. 16h - EEE Wake Error Register
- Device ID = 07h, Reg. 3Ch - EEE Advertisement Register
- Device ID = 07h, Reg. 3Dh - EEE LP Advertisement Register
- Device ID = 07h, Reg. 3Fh - EEE Message Code Register

Wake on LAN (WOL)

Wake on LAN is normally a MAC based feature to wake up a host system (a PC for example) when special packets are received and detected. The packet is typically sent by a remote administrator. The KSZ9031RNX can perform the same function if the MAC address of its associated MAC device is copied into the PHY device.

The resources available for this feature includes the PME_N interrupt signal and a collection of register bits. The PME_N signal is available on either the INT_N/PME_N pin (pin 38) or on the LED 1/PHYAD0/PME_N pin (pin 17). The selection of pins is accomplished via the strapping options. Strapping option “1010” places the PME_N signal on the INT_N pin. Strapping option “1000” places the PME_N signal on the LED1 pin. See the Strapping Options section for more information. The status of the PME_N signal is available via the PMEN_OUT bit at MMD Device 2h, Reg. 10h, bit 15.

There are three events that will trigger an event on PME_N; detection of a Magic Packet, detection of a Custom Packet, or a Linkup condition. Their configuration and usage are described below.

"Magic Packet" Detection

- The Magic Packet consists of six bytes of FFh followed by sixteen repetitions of the units MAC Address.
- The MAC Address is specified in Device 2h, Reg. 11h, 12h, 13h.
- The detection of the Magic Packet is enabled by setting Device 2h, Reg. 10h, bit 1.

Customized Packet Detection

- Four sets of Customized Packets to support four different types of Wake Up scenarios
- As the Customized Packet is received, its CRC is calculated and compared to the CRC value that is stored in registers for that particular Custom Packet.
- Each Customized Packet has associate with it a set of Mask bits to indicate which bits/bytes to utilize in the CRC calculation.
- The 32 bits of expected CRC for each of the four Customized Packets are stored in Device 2h, Reg. 14h – 1Bh.
- The Mask bits for each of the four Customized Packets are stored in Device 2h, Reg. 1Ch – 2Bh.
- Each of the four Customized Packets are enabled via Device 2h, Reg. 10h, bits [5:2].
- The received CRC bits for each of the four Customized Packets are stored in Device 2h, Reg. 30h – 37h.

Link Up Detection

- Transitioning from a Link Down condition to a valid Link Up condition will generate the PME_N event.

Typical Current / Power Consumption

The following tables show the typical current consumption by the core (DVDDL, AVDDL, AVDDL_PLL), transceiver (AVDDH) and digital I/Os (DVDDH) supply pins, and the total typical power for the entire KSZ9031RNX device for various nominal operating voltages combinations.

Transceiver (3.3V), Digital I/Os (3.3V)

Condition	1.2V Core	3.3V Transceiver (AVDDH)	3.3V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	64.7	22.0	540
1000Base-T Full-duplex @ 100% utilization	222	63.7	42.4	620
100Base-TX Link-up (no traffic)	61.8	27.3	15.4	215
100Base-TX Full-duplex @ 100% utilization	62.1	27.3	17.5	225
10Base-T Link-up (no traffic)	6.8	14.2	10.9	92
10Base-T Full-duplex @ 100% utilization	7.3	24.8	11.0	130
EEE Mode – 1000Mbps	24.8	4.7	5.0	65
EEE Mode – 100Mbps	24.9	17.5	5.0	105
Software Power Down Mode (Reg. 0h.11 =1)	1.1	3.4	10.6	50

Transceiver (2.5V), Digital I/Os (2.5V)

Condition	1.2V Core	2.5V Transceiver (AVDDH)	2.5V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	56.4	14.7	430
1000Base-T Full-duplex @ 100% utilization	222	55.4	31.0	485
100Base-TX Link-up (no traffic)	61.8	23.2	11.1	160
100Base-TX Full-duplex @ 100% utilization	62.1	23.2	12.9	165
10Base-T Link-up (no traffic)	6.8	10.0	7.9	55
10Base-T Full-duplex @ 100% utilization	7.3	21.5	8.1	85
EEE Mode – 1000Mbps	24.8	3.4	4.0	50
EEE Mode – 100Mbps	24.9	14.6	4.0	80
Software Power Down Mode (Reg. 0h.11 =1)	1.1	2.1	6.7	25

Transceiver (2.5V), Digital I/Os (1.8V)

Condition	1.2V Core	2.5V Transceiver (AVDDH)	1.8V Digital I/Os (DVDDH)	Total Chip Power
	mA	mA	mA	mW
1000Base-T Link-up (no traffic)	210	56.4	11.2	415
1000Base-T Full-duplex @ 100% utilization	222	55.4	23.5	450
100Base-TX Link-up (no traffic)	61.8	23.2	8.3	150
100Base-TX Full-duplex @ 100% utilization	62.1	23.2	9.6	150
10Base-T Link-up (no traffic)	6.8	10.0	5.8	45
10Base-T Full-duplex @ 100% utilization	7.3	21.5	6.0	75
EEE Mode – 1000Mbps	24.8	3.4	4.0	50
EEE Mode – 100Mbps	24.9	14.6	4.0	75
Software Power Down Mode (Reg. 0h.11 =1)	1.1	2.1	4.6	15

Register Map

The register space within the KSZ9013RN is comprised of two distinct areas. The first area is compliant to the IEEE 802.3 Specification. This provides a standard 32-register address space for the PHY. Registers 0 thru 15 are standard PHY registers, defined per the specification. Registers 16 thru 31 are vendor specific registers.

The second area is comprised of the MMD registers. The MMD registers are accessed indirectly via two portal registers; the MMD Setup Register (Reg. 0Dh) and the MMD Index/Data Register (Reg. 0Eh).

The MMD register set is defined in Section 22 of the IEEE 802.3 2005 specification. The MMD registers consist of up to 64 devices with each device supporting up to 65536 16 bit registers.

Access is indirect using register 0Dh and 0Eh. 0Dh determines if the access is being used to set the register address or is a data access. Register 0Eh contains either the register address, or read/write data.

The overall register summary is shown in Table 9.

Examples:

- MMD Register Read // Read from Customized-Pkt-0-Mask-HH Register

1. Write 0002h to MMD Setup Register (Reg. Dh) // Set ID = 02h, set OP Mode = “00” = Reg. Index
2. Write 001fh to MMD Data Register (Reg. Eh) // Load the Reg. Index for the Cust.-Pkt-0-HH Reg
3. Write 8002h to MMD Setup Register (Reg. Dh) // Set ID = 02h, set OP Mode = “10”, Post Inc. Read OP
4. Read Reg. data via MMD Data Register (Reg. Eh) // Read Reg. Data via MMD Data Register

- MMD Register Write // Write to Wake On LAN Control Register

1. Write 0002h to MMD Setup Register (Reg. Dh) // Set ID = 02h, set OP Mode = “00” = Reg. Index
2. Write 0010h to MMD Data Register (Reg. Eh) // Load the Reg. Index for the WOL Control Reg
3. Write c002h to MMD Setup Register (Reg. Dh) // Set ID = 02h, set OP Mode = “11”, Post Inc. Write OP
4. Write “WR” data to MMD Data Register (Reg. Eh) // Load “WR” Data into MMD Data Register

Register Number (Hex)	Description
IEEE Defined Registers	
0h (0d)	Basic Control Register
1h (1d)	Basic Status Register
2h (2d)	PHY Identifier 1 Register
3h (3d)	PHY Identifier 2 Register
4h (4d)	Auto-Negotiation Advertisement Register
5h (5d)	Auto-Negotiation Link Partner Ability Register
6h (6d)	Auto-Negotiation Expansion Register
7h (7d)	Auto-Negotiation Next Page
8h (8d)	Auto-Negotiation Link Partner Next Page Ability Register
9h (9d)	1000Base-T Control Register
Ah (10d)	1000Base-T Status Register
Bh (11d)	(Reserved)
Ch (12d)	(Reserved)
Dh (13d)	MMD Setup Register
Eh (14d)	MMD Index/Data Register
Fh (15d)	Extended – MII Status
Vendor Specific Registers	

Register Number (Hex)	Description
10h (16d)	Reserved
11h (17d)	PCS Loopback Swap/Polarity Control Register
12h (18d)	Cable Diagnostic Register
13h (19d)	Digital PMA/PCS Status Register
14h (20d)	Digital AX/AN Status Register
15h (21d)	RXER Counter Register
16h (22d) – 1Ah (26d)	Reserved
1Bh (27d)	Interrupt Control/Status Register
1Ch (28d)	Digital Debug Control 1 Register
1Dh (29d)	Reserved
1Eh (30d)	Reserved
1Fh (31d)	PHY Control Register
MMD Registers	
Device ID 2h, Reg. 0h	Common Control Register
Device ID 2h, Reg. 1h	Strap Status Register
Device ID 2h, Reg. 2h	Operation Mode Strap Override Register
Device ID 2h, Reg. 3h	Operation Mode Strap Status Register
Device ID 2h, Reg. 5h	RX Data Pad Skew Register
Device ID 2h, Reg. 6h	TX Data Pad Skew Register
Device ID 2h, Reg. 8h	Clock Pad Skew Register
Device ID 2h, Reg. 10h	Wake On LAN Control Register
Device ID 2h, Reg. 11h – 13h	WOL MAC Address [47:00] Registers
Device ID 2h, Reg. 14h – 1Bh	WOL Customized Packet[1:0] Expected CRC[31:00] Registers
Device ID 2h, Reg. 1Ch – 2Bh	WOL Customized Packet[1:0] Mask[63:00] Registers
Device ID 2h, Reg. 30h – 37h	WOL Customized Packet[1:0] Received CRC[31:00] Registers
Device ID 3h, Reg. 0h	PCS Register
Device ID 3h, Reg. 1h	PCS EEE Status Register
Device ID 3h, Reg. 14h	EEE Cap Status Register
Device ID 3h, Reg. 16h	EEE Wake Error Count Register
Device ID 7h, Reg. 3Ch	EEE Advertisement Register
Device ID 7h, Reg. 3Dh	EEE LP Advertisement Register
Device ID 7h, Reg. 3Fh	EEE Message Code Register
Device ID 28h, Reg.0h	Analog Control 0 Register
Device ID 28h, Reg.7h	EDPD Control Register

Table 9 Overall KSZ9031RNX Register Summary

Register Descriptions

IEEE Defined Registers

The information in this section describes the registers and the bits for the IEEE Defined Registers as implemented in the KSZ9031RNX.

Address	Name	Description	Mode[1]	Default
Register 0 (0h) – Basic Control				
0.15	Reset	1 = Software PHY reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loop-back	1 = Loop-back mode 0 = Normal operation	RW	0
0.13	Speed Select (LSB)	[0.6, 0.13] [1,1] = Reserved [1,0] = 1000 Mbps [0,1] = 100 Mbps [0,0] = 10 Mbps This bit is ignored if Auto-Negotiation is enabled (Reg. 0h.12 = 1).	RW	Hardware Setting
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation process 0 = Disable Auto-Negotiation process If enabled, Auto-Negotiation result overrides settings in Reg. 0h.13, 0.8 and 0.6.	RW	1
0.11	Power Down	1 = Power down mode 0 = Normal operation	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from GMII/MII 0 = Normal operation	RW	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Hardware Setting
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6	Speed Select (MSB)	[0.6, 0.13] [1,1] = Reserved [1,0] = 1000 Mbps [0,1] = 100 Mbps [0,0] = 10 Mbps This bit is ignored if Auto-Negotiation is enabled (Reg. 0h.12 = 1).	RW	0
0.5:0	Reserved		RO	00_0000
Register 1 (1h) – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full Duplex	1 = Capable of 100 Mbps full-duplex 0 = Not capable of 100 Mbps full-duplex	RO	1

Address	Name	Description	Mode[1]	Default
1.13	100Base-TX Half Duplex	1 = Capable of 100 Mbps half-duplex 0 = Not capable of 100 Mbps half-duplex	RO	1
1.12	10Base-T Full Duplex	1 = Capable of 10 Mbps full-duplex 0 = Not capable of 10 Mbps full-duplex	RO	1
1.11	10Base-T Half Duplex	1 = Capable of 10 Mbps half-duplex 0 = Not capable of 10 Mbps half-duplex	RO	1
1.10:9	Reserved	Reserved	RO	00
1.8	Extended Status	1 = Extended Status Information in Reg. 15. 0 = No Extended Status Information in Reg. 15.	RO	1
1.7	Reserved	Reserved	RO	0
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform Auto-Negotiation 0 = Not capable to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1
Register 2 (2h) – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1h	RO	0022h
Register 3 (3h) – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1h	RO	0001_01
3.9:4	Model Number	Six-bit manufacturer's model number	RO	10_0001
3.3:0	Revision Number	Four-bit manufacturer's revision number	RO	Indicates silicon revision
Register 4 (4h) – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
4.14	Reserved	Reserved	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	Reserved	RO	0

Address	Name	Description	Mode[1]	Default
4.11:10	Pause	[4.11, 4.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device)	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	1
4.7	100Base-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RW	1
4.6	10Base-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5 (5h) – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved	Reserved	RO	0
5.11:10	Pause	[5.11, 5.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device)	RW	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100 Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0000
Register 6 (6h) – Auto-Negotiation Expansion				

Address	Name	Description	Mode[1]	Default
6.15:5	Reserved	Reserved	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has Auto-Negotiation capability 0 = Link partner does not have Auto-Negotiation capability	RO	0
Register 7 (7h) – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved	Reserved	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8 (8h) – Auto-Negotiation Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field		RO	000_0000_0000
Register 9 (9h) – 1000Base-T Control				

Address	Name	Description	Mode[1]	Default
9:15:13	Test Mode Bits	Transmitter test mode operations [9.15:13] Mode [000] Normal Operation [001] Test mode 1 –Transmit waveform test [010] Test mode 2 –Transmit jitter test in Master mode [011] Test mode 3 –Transmit jitter test in Slave mode [100] Test mode 4 –Transmitter distortion test [101] Reserved, operations not identified [110] Reserved, operations not identified [111] Reserved, operations not identified	RW	000
9.12	MASTER-SLAVE Manual Config Enable	1 = Enable MASTER-SLAVE Manual configuration value 0 = Disable MASTER-SLAVE Manual configuration value	RW	0
9.11	MASTER-SLAVE Manual Config Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation This bit is ignored if MASTER-SLAVE Manual Config is disabled (Reg. 9.12 = 0).	RW	0
9.10	Port Type	1 = Indicate the preference to operate as multiport device **(MASTER)** 0 = Indicate the preference to operate as single-port device (**SLAVE**) This bit is valid only if the MASTER-SLAVE Manual Config Enable bit is disabled (register 9.12 = 0).	RW	0
9.9	1000Base-T Full-Duplex	1 = Advertise PHY is 1000Base-T full-duplex capable 0 = Advertise PHY is not 1000Base-T full-duplex capable	RW	1
9.8	1000Base-T Half-Duplex	1 = Advertise PHY is 1000Base-T half-duplex capable 0 = Advertise PHY is not 1000Base-T half-duplex capable	RW	Hardware Setting
9.7:0	Reserved	Write as 0, ignore on read	RO	
Register 10 (Ah) – 1000Base-T Status				
10.15	MASTER-SLAVE configuration fault	1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC	0

Address	Name	Description	Mode[1]	Default
10.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO	0
10.13	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status = 1) 0 = Local Receiver not OK (loc_rcvr_status = 0)	RO	0
10.12	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status = 1) 0 = Remote Receiver not OK (rem_rcvr_status = 0)	RO	0
10.11	LP 1000T FD	1 = Link Partner is capable of 1000Base-T full-duplex 0 = Link Partner is not capable of 1000Base-T full-duplex	RO	0
10.10	LP 1000T HD	1 = Link Partner is capable of 1000Base-T half-duplex 0 = Link Partner is not capable of 1000Base-T half-duplex	RO	0
10.9:8	Reserved	Reserved	RO	00
10.7:0	Idle Error Count	Cumulative count of errors detected when receiver is receiving idles and PMA_TXMODE.indicate = SEND_N. The counter is incremented every symbol period that rxerror_status = ERROR.	RO/SC	0000_0000
Register 11 (Bh) – Reserved				
11.15:0	Reserved	Reserved	RW	0000_0000_0000_0000
Register 12 (Ch) – Reserved				
12.15:0	Reserved	Reserved	RW	0000_0000_0000_0000
Register 13 (Dh) – MMD Setup Register				
13.15:14	MMD Operation Mode	These two bits determine the type of MMD operation and also the usage of the MMD Data Register (Reg. 0Eh). 00: Register Index is in Reg. 0Eh. 01: Data OP without post-index increment 10: Data OP with post-index increment on R/W 11: Data OP with post-index increment on W	RW	0000_0000_0000_0000
13.13:6	Reserved	Reserved	RW	0
13.5:0	MMD Device ID	These bits determine the value of the Device ID (0-31) for the current MMD register R/W.	RW	00_0000
Register 14 (Eh) – MMD Data Register				

Address	Name	Description	Mode[1]	Default
14.15:0	MMD R/W Index/Data	When Reg. 0Dh = 00h, this register is used for the Index value for the MMD R/W operation. Otherwise, this register is the R/W data for the MMD R/W operation.	RW	0000_0000_0000_0000
Register 15 (Fh) – Extended – MII Status				
15.15	1000Base-X Full-duplex	1 = PHY able to perform 1000Base-X full-duplex 0 = PHY not able to perform 1000Base-X full-duplex	RO	0
15.14	1000Base-X Half-duplex	1 = PHY able to perform 1000Base-X half-duplex 0 = PHY not able to perform 1000Base-X half-duplex	RO	0
15.13	1000Base-T Full-duplex	1 = PHY able to perform 1000Base-T full-duplex 1000BASE-X 0 = PHY not able to perform 1000Base-T full-duplex	RO	1
15.12	1000Base-T Half-duplex	1 = PHY able to perform 1000Base-T half-duplex 0 = PHY not able to perform 1000Base-T half-duplex	RO	1
15.11:0	Reserved	Ignore when read	RO	-

Note:

1. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

Vendor Specific Registers

Address	Name	Description	Mode[1]	Default
Register 17 (11h) – Remote Loopback, LED Mode				
17.15:9	Reserved	Reserved	RW	0000_001
17.8	Remote Loopback	1 = Enable Remote Loopback 0 = Disable Remote Loopback	RW	0
17.7:6	Reserved	Reserved	RW	11
17.5:4	Reserved	Reserved	RW	11
17.3	LED Test Enable	1 = Enable LED test mode 0 = Disable LED test mode	RW	0
17.2:1	Reserved	Reserved	RW	00
17.0	Reserved	Reserved	RO	0

Address	Name	Description	Mode[1]	Default
Register 18 (12h) – LinkMD® – Cable Diagnostic				
18.15	Reserved	Reserved	RW/SC	0
18.14:8	Reserved	Reserved	RW	000_0000
18.7:0	Reserved	Reserved	RO	0000_0000
Register 19 (13h) – Digital PMA/PCS Status				
19.15:3	Reserved	Reserved	RO/LH	0000_0000_0000_0
19.2	1000Base-T Link Status	1000 Base-T Link Status 1 = Link status is OK 0 = Link status is not OK	RO	0
19.1	100Base-TX Link Status	100 Base-TX Link Status 1 = Link status is OK 0 = Link status is not OK	RO	0
19.0	Reserved	Reserved	RO	0
Register 21 (15h) – RXER Counter				
21.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/RC	0000_0000_0000_0000
Register 27 (1Bh) – Interrupt Control/Status				
27.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
27.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
27.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
27.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
27.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
27.10	Link Down Interrupt Enable	1 = Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
27.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
27.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
27.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occurred	RO/RC	0
27.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occurred	RO/RC	0

Address	Name	Description	Mode[1]	Default
27.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occurred	RO/RC	0
27.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occurred	RO/RC	0
27.3	Link Partner Acknowledge Interrupt	1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occurred	RO/RC	0
27.2	Link Down Interrupt	1 = Link Down occurred 0 = Link Down did not occurred	RO/RC	0
27.1	Remote Fault Interrupt	1 = Remote Fault occurred 0 = Remote Fault did not occurred	RO/RC	0
27.0	Link Up Interrupt	1 = Link Up occurred 0 = Link Up did not occurred	RO/RC	0
Register 28 (1Ch) – Digital Debug Control 1				
28.15:8	Reserved	Reserved	RW	0000_0000
28.7	mdi_set	mdi_set has no function when swapoff (Reg. 28, bit 6) is de-asserted. 1 = When swapoff is asserted, if mdi_set is asserted, chip will operate at MDI mode. 0 = When swapoff is asserted, if mdi_set is de-asserted, chip will operate at MDI-X mode.	RW	0
28.6	swapoff	1 = Disable auto crossover function 0 = Enable auto crossover function	RW	0
28.5:1	Reserved	Reserved	RW	00_000
28.0	PCS Loopback	1 = Enable 10Base-T and 100Base-TX Loopback for Reg. 0h bit 14. 0 = normal function	RW	0
Register 31 (1Fh) – PHY Control				
31.15	Reserved	Reserved	RW	0
31.14	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
31.13:12	Reserved	Reserved	RW	00
31.11:10	Reserved	Reserved	RO/LH/RC	00
31.9	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
31.8:7	Reserved	Reserved	RW	00
31.6	Speed status 1000Base-T	1 = Indicate chip final speed status at 1000Base-T	RO	0
31.5	Speed status 100Base-TX	1 = Indicate chip final speed status at 100Base-TX	RO	0
31.4	Speed status 10Base-T	1 = Indicate chip final speed status at 10Base-T	RO	0

Address	Name	Description	Mode[1]	Default
31.3	Duplex status	Indicate chip duplex status 1 = Full-duplex 0 = Half-duplex	RO	0
31.2	1000Base-T Mater/Slave status	1 = Indicate 1000Base-T Master mode 0 = Indicate 1000Base-T Slave mode	RO	0
31.1	Software Reset	1 = Reset chip, except all registers 0 = Disable reset	RW	0
31.0	Link Status Check Fail	1 = Fail 0 = Not Failing	RO	0

Note:

1. RW = Read/Write.
   RC = Read-cleared
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.

MMD Registers

The information in this section describes the registers and the bits for the MMD Registers as implemented in the KSZ9031RNX. The overall layout of the MMD Registers are shown in Table 10.

MMD Device Name	ID	Registers Used
Common Control Registers	2h	00h - 03h, 10h – 2Bh
EEE_WOL Register	3h	14h, 16h
EEE Advertise Register	7h	3Ch, 3Dh, 3Fh
AFED Register	28h	00h, 23h

Table 10 MMD Register Summary

MMD Device ID = 2h (2d): Common Control Registers

Register 16'h0 (0)– Common Control Register				
Address	**Name**	**Description**	**Attribute**	**Default**
2.0.15:0	Reserved	Reserved	RW	6'b0
2.0.9	Cr_tx_er disable	1 = disable TX ER signal 0 = normal function	RW	1'h0
2.0.8	Cr_phy_status_en	1 = Enable RGMII in band PHY status 0 = Disable	RW	1'h0
2.0.7:5	PRBS order		RW	3'b0
2.0.4	Single LED		RW	Hardware Strap
2.0.3	Reserved	Reserved	RW	1'b0
2.0.2	Reserved	Reserved	RW	Hardware Strap

2.0.1	clk125 Enable		RW	Hardware Strap
2.0.0	All-PHYAD Enable		RW	1'b0
Register 16'h1 (1)– Strap Status Register				
2.1.15:8	Reserved	Reserved	RO	8'h0
2.1.7	Strap_led_single	Strap status of single LED	RO	Hardware Strap
2.1.6	Reserved	Reserved	RO	
2.1.5	strap_clk125en2reg	Strap status of clk125_ndo PAD enable	RO	
2.1.4:0	strap_phyad[4:0]	PHY Address	RO	
Register 16'h2 (2)– Operation Mode Strap Override Register				
2.2.15	Cr_an_all_cap	Override strap advertise all capabilities (RGMII)	RW	Hardware Strap
2.2.14	Cr_an_all_ng_h_cap	Override strap advertise all capabilities except 1000T half duplex (RGMII)	RW	
2.2.13	Cr_an_g_fh_cap	Override strap advertise 1000T full and half-duplex only (RGMII)	RW	
2.2.12	Cr_an_g_f_cap	Override strap advertise 1000T full duplex only (RGMII)	RW	
2.2.11	Reserved	Reserved	RW	
2.2.10	Ovr_PME_N_INT_N	Overide RGMII PME_N/INT_N Strap Mode ["1010"]	RW	
2.2.9	Reserved	Reserved	RW	Hardware Strap
2.2.8	Ovr_PME_N_LED1	Overide RGMII PME_N/ILED1 Strap Mode ["1000"]	RW	Hardware Strap
2.2.7	Ovr_IDDQ	Overide IDDQ / Power Down Strap Mode ["0111"] status	RW	
2.2.6	Reserved	Reserved	RW	
2.2.5	Reserved	Reserved	RW	
2.2.4	Ovr_NAND_Tree	Overide NAND tree mode Strap Mode ["0100"] status	RW	
2.2.3	Reserved	Reserved	RW	
2.2.2	Reserved	Reserved	RW	
2.2.1	Reserved	Reserved	RW	
2.2.0	Ovr_RGMII	Overide RGMII mode Strap Mode ["0000"] status	RW	
Register 16'h3h (3)– Operation Mode Strap Status Register				
2.3.15	Strap_an_all_cap	Strap advertise all capabilities (RGMII)	RO	Hardware Setting
2.3.14	Strap_an_all_ng_h_cap	Strap advertise all capabilities except 1000T half duplex (RGMII)	RO	
2.3.13	Strap_an_g_fh_cap	Strap advertise 1000T full and half-duplex only (RGMII)	RO	
2.3.12	Strap_an_g_f_cap	Strap advertise 1000T full duplex only (RGMII)	RO	
2.3.11	Reserved	Reserved	RO	
2.3.10	Strap_PME_N_INT_N	RGMII PME_N/INT_N Strap Mode ["1010"]	RO	
2.3.9	Reserved	Reserved	RO	
2.3.8	Strap_PME_N_LED1mode	RGMII PME_N/ILED1 Strap Mode ["1010"]	RO	
2.3.7	Strap_iddq_mode	IDDQ / Power Down Strap Mode ["0111"] status	RO	
2.3.6	Reserved	Reserved	RO	
2.3.5	Reserved	Reserved	RO	

2.3.4	Strap_ntree_mode	NAND tree mode Strap Mode [“0100”] status	RO	
2.3.3	Reserved	Reserved	RO	
2.3.2	Reserved	Reserved	RO	
2.3.1	Reserved	Reserved	RO	
2.3.0	Strap_RGMII_Mode	RGMII mode Strap Mode [“0000”] status	RO	
Register 16’h4 (4)– Reserved				
2.4.15:0	Reserved	Reserved	RW	4’h0
Register 16’h5 (5)– RX Data Pad Skew Register				
2.5.15:12	rxd3_pad_skew	RXD3 PAD output Skew Control (0.12ns/step)	RW	4’h7
2.5.11:8	rxd2_pad_skew	RXD2 PAD output Skew Control (0.12ns/step)	RW	4’h7
2.5.7:4	rxd1_pad_skew	RXD1 PAD output Skew Control (0.12ns/step)	RW	4’h7
2.5.3:0	rxd0_pad_skew	RXD0 PAD output Skew Control (0.12ns/step)	RW	4’h7
Register 16’h6(6)-TX Data Pad Skew Register				
2.6.15:12	Txd3_pad_skew	TXD3 PAD input Skew Control(0.12ns/step)	RW	4’h7
2.6.11:8	Txd2_pad_skew	TXD2 PAD input Skew Control(0.12ns/step)	RW	4’h7
2.6.7:4	Txd1_pad_skew	TXD1 PAD input Skew Control(0.12ns/step)	RW	4’h7
2.6.3:0	Txd0_pad_skew	TXD0 PAD input Skew Control(0.12ns/step)	RW	4’h7
Register 16’h7(7)-Reserved				
2.7.15:0	Reserved	Reserved	RW	16’h0
Register 16’h8(8)-Clock-PAD Skew Register				
2.8.15	Reserved	Reserved	RW	1’h0
2.8.14:10	Txc_pad_oskew	TXC PAD output Skew Control(0.12ns/step)	RW	5’h0f
2.8.9:5	GTxc_pad_iskew	GTXC PAD input Skew Control(0.12ns/step)	RW	5’h0f
2.8.4:0	Rxc_pad_oskew	RXC PAD output Skew Control(0.12ns/step)	RW	5’h0f
Register 16’h9(9)-Reserved				
2.9.15:11	Reserved	Reserved	RW	Hardware Strap
2.9.10:0	Reserved	Reserved	RW	11’h1ff
Register 16’hA(10)-Reserved				
2.10.15.10	Reserved	Reserved	RW	6’h0
2.10.9:0	Reserved	Reserved	RW	10’h10
Register 16’hB(11)-Reserved				
2.11.15:0	Reserved	Reserved		2’b0
Register 16’hC(12)-Reserved				
2.12.15:0	Reserved	Reserved	RO	16’h0
Register 16’hD(13)-Reserved				
2.13.15:0	Reserved	Reserved	RO	16’h0
Register 16’hE(14)-Reserved				
2.14.15:0	Reserved	Reserved	RO	16’h0
Register 16’hF(15)-Reserved				
2.15.15:0	Reserved	Reserved		16’h0
Register 16’h10(16)-Wake-On-Lan Control Register				

2.16.15	Pmen_out	Status of PMEN_OUT	RO	1'b1
2.16.14:6	Reserved	Reserved		9'h0
2.16.5:2	En_cpkt_pmen	Enable Wake-On-LAN with Customized Packet type 0-3	RW	4'h0
2.16.1	En_mpkt_pmen	Enable Wake-On-LAN with Magic Packet	RW	1'b0
2.16.0	En_link_pmen	Enable Wake-On-LAN with Link up	RW	1'b0
Register 16'h11(17)-Wake-On-Lan-MAC-LO Register				
2.17.15:0	m-pkt-mac-lo	MAC-Address[15:0] of magic packet	RW	16'h0
Register 16'h12(18)-Wake-On-Lan-MAC-MI Register				
2.18.15:0	m-pkt-mac-mi	MAC-Address[31:16] of magic packet	RW	16'h0
Register 16'h13(19)-Wake-On-Lan-MAC-HI Register				
2.19.15:0	m-pkt-mac-hi	MAC-Address[47:32] of magic packet	RW	16'h0
Register 16'h14(20)-Customized-Pkt-0-CRC-LO Register				
2.20.15:0	c-pkt-0-crc-lo	C-PKT-0 CRC[15:0]	RW	16'h0
Register 16'h15(21)-Customized-Pkt-0-CRC-HI Register				
2.21.15:0	c-pkt-0-crc-hi	C-PKT-0 CRC[31:16]	RW	16'h0
Register 16'h16(22)-Customized-Pkt-1-CRC-LO Register				
2.22.15:0	c-pkt-1-crc-lo	C-PKT-0 CRC[15:0]	RW	16'h0
Register 16'h17(23)-Customized-Pkt-1-CRC-HI Register				
2.23.15:0	c-pkt-1-crc-hi	C-PKT-0 CRC[31:16]	RW	16'h0
Register 16'h18(24)-Customized-Pkt-2-CRC-LO Register				
2.24.15:0	c-pkt-2-crc-lo	C-PKT-0 CRC[15:0]	RW	16'h0
Register 16'h19(25)-Customized-Pkt-2-CRC-HI Register				
2.25.15:0	c-pkt-2-crc-hi	C-PKT-0 CRC[31:16]	RW	16'h0
Register 16'h1A(26)-Customized-Pkt-3-CRC-LO Register				
2.26.15:0	c-pkt-3-crc-lo	C-PKT-0 CRC[15:0]	RW	16'h0
Register 16'h1B(27)-Customized-Pkt-3-CRC-HI Register				
2.27.15:0	c-pkt-3-crc-hi	C-PKT-0 CRC[31:16]	RW	16'h0
Register 16'h1C(28)-Customized-Pkt-0-MASK_LL Register				
2.28.15:0	c-pkt-0-mask-ll	C-PKT-0 mask[15:0]	RW	16'h0
Register 16'h1D(29)-Customized-Pkt-0-MASK-LH Register				
2.29.15:0	c-pkt-0-mask-lh	C-PKT-0 mask[31:16]	RW	16'h0
Register 16'h1E(30)-Customized-Pkt-0-MASK-HL Register				
2.30.15:0	c-pkt-0-mask-hl	C-PKT-0 mask[47:32]	RW	16'h0
Register 16'h1F31)-Customized-Pkt-0-MASK-HH Register				
2.31.15:0	c-pkt-0-mask-hh	C-PKT-0 mask[63:48]	RW	16'h0
Register 16'h20(32)-Customized-Pkt-1-MASK_LL Register				
2.32.15:0	c-pkt-1-mask-ll	C-PKT-1 mask[15:0]	RW	16'h0
Register 16'h21(33)-Customized-Pkt-1-MASK-LH Register				
2.33.15:0	c-pkt-1-mask-lh	C-PKT-1 mask[31:16]	RW	16'h0
Register 16'h22(34)-Customized-Pkt-1-MASK-HL Register				
2.34.15:0	c-pkt-1-mask-hl	C-PKT-1 mask[47:32]	RW	16'h0

Register 16'h23(35)-Customized-Pkt-1-MASK-HH Register				
2.35.15:0	c-pkt-1-mask-hh	C-PKT-1 mask[63:48]	RW	16'h0
Register 16'h24(36)-Customized-Pkt-2-MASK_LL Register				
2.36.15:0	c-pkt-2-mask-ll	C-PKT-2 mask[15:0]	RW	16'h0
Register 16'h25(37)-Customized-Pkt-2-MASK-LH Register				
2.37.15:0	c-pkt-2-mask-lh	C-PKT-2 mask[31:16]	RW	16'h0
Register 16'h26(38)-Customized-Pkt-2-MASK-HL Register				
2.38.15:0	c-pkt-2-mask-hl	C-PKT-2 mask[47:32]	RW	16'h0
Register 16'h27(39)-Customized-Pkt-2-MASK-HH Register				
2.39.15:0	c-pkt-2-mask-hh	C-PKT-2 mask[63:48]	RW	16'h0
Register 16'h28(40)-Customized-Pkt-3-MASK_LL Register				
2.40.15:0	c-pkt-3-mask-ll	C-PKT-3 mask[15:0]	RW	16'h0
Register 16'h29(41)-Customized-Pkt-3-MASK-LH Register				
2.41.15:0	c-pkt-3-mask-lh	C-PKT-3 mask[31:16]	RW	16'h0
Register 16'h2A(42)-Customized-Pkt-3-MASK-HL Register				
2.42.15:0	c-pkt-3-mask-hl	C-PKT-3 mask[47:32]	RW	16'h0
Register 16'h2B(43)-Customized-Pkt-3-MASK-HH Register				
2.43.15:0	c-pkt-3-mask-hh	C-PKT-3 mask[63:48]	RW	16'h0
Register 16'h2C(44)-Wake-On_LAN Control Status Register				
2.44.15:0	Wol_ctrl_status	Wake-on-Lan Control Module Status	RO	16'h0
Register 16'h2D(45)-Wake-On_LAN Custom Packet Receive Status Register				
2.45.15:0	Wol_cpkt_status	Wake-on-Lan Custom Packet Receive Status	RO	16'h0
Register 16'h2E(46)-Wake-On_LAN Magic Packet Receive Status Register				
2.46.15:0	Wol_mpkt_status	Wake-on-Lan Magic Packet Receive Status	RO	16'h0
Register 16'h2F(47)-Wake-On_LAN Data Module Status Register				
2.47.15:0	Wol_data_status	Wake-on-Lan Data Module Status	RO	16'h0
Register 16'h30(48)-Customized Pkt-0 Received CRC-L Register				
2.48.15:0	Wol_crc_rcv_0 [15:0]	WoL CRC [15:0] calculated on C-PKT-0	RO	16'hffff
Register 16'h31(49)-Customized Pkt-0 Received CRC-H Register				
2.49.15:0	Wol_crc_rcv_0 [31:16]	WoL CRC [31:16] calculated on C-PKT-0	RO	16'hffff
Register 16'h32(50)-Customized Pkt-1 Received CRC-L Register				
2.50.15:0	Wol_crc_rcv_1 [15:0]	WoL CRC [15:0] calculated on C-PKT-1	RO	16'hffff
Register 16'h33(51)-Customized Pkt-1 Received CRC-H Register				
2.51.15:0	Wol_crc_rcv_1 [31:16]	WoL CRC [31:16] calculated on C-PKT-1	RO	16'hffff
Register 16'h34(52)- Customized Pkt-2 Received CRC-L Register				
2.52.15:0	Wol_crc_rcv_2 [15:0]	WoL CRC [15:0] calculated on C-PKT-2	RO	16'hffff
Register 16'h35(53)- Customized Pkt-2 Received CRC-H Register				
2.53.15:0	Wol_crc_rcv_2 [31:16]	WoL CRC [31:16] calculated on C-PKT-2	RO	16'hffff
Register 16'h36(54)- Customized Pkt-3 Received CRC-L Register				
2.54.15:0	Wol_crc_rcv_3 [15:0]	WoL CRC [15:0] calculated on C-PKT-3	RO	16'hffff
Register 16'h37(55)- Customized Pkt-3 Received CRC-H Register				

2.55.15:0	Wol_crc_rcv_3 [31:16]	WoL CRC [31:16] calculated on C-PKT-3	RO	16'hffff

MMD Device ID = 3h (3d): **EEE_WOL Register**

Register 16'h0 (0)– PCS Register				
3.0.15:0	Reserved	Reserved	RW	16'b0
Register 16'h1 (1)– PCS EEE-Status Register				
3.1.15:0	Reserved	Reserved		16'b0
Register 16'h14 (20)– EEE-Cap-Status Register				
3.20.15:7	Reserved	Reserved		9'b0
3.20.6:3	Reserved	Reserved	RO	4'b0
3.20.2	1000BASE-T EEE	1= EEE is supported for 1G BaseT	RO	1'b0
3.20.1	100BASE-TX EEE	1= EEE is supported for 100 BaseT	RO	1'b0
3.20.0	Reserved	Reserved		1'b0
Register 16'h16 (22)– EEE-Wake-Error Register				
3.20.15:0	EEE_Wake_Error_Cnt	EEE wake error counter This counter counts the faults that have occurred when the PHY fails to complete normal wake up sequence within the required time.	RW	16'b0

MMD Device ID = 7h (7d): **EEE Advertise Register**

Register 16'h3c (60) – EEE Advertisement Register				
Address	**Name**	**Description**	**Attribute**	**Default**
7.60.15:11	Reserved	Reserved		5'h0
7.60.10:0	EEE_adv	Bit [2] for 1G-EEE, B1 for 100-EEE	RW	11'h006
Register 16'h3d (61)– EEE LP advertisement Register				
7.61.15:11	Reserved	Reserved		5'h0
7.61.10:0	EEE_lp_adv	Bit [2] for 1G-EEE, B1 for 100-EEE	RO	11'h000
Register 16'h3f (63)– EEE message code Register				
7.63.15:11	Reserved	Reserved		5'h0
7.63.10:0	EEE_message_code	Programmable EEE specific message code for AN	RW	11'h00A

MMD Device ID = 28h (40d): AFED Register

Register 0h (0) – Analog Control Register 0				
Address	**Name**	**Description**	**Attribute**	**Default**
40.0.15:0	dgt_afe_reg0[15:0]		RW	16'h0000
40.0.15	LDO_dis	Allow turning off VDD regulator via software 0: On (Default) 1: Off	RW	1'h0
40.0.14:12	Reserved	Reserved	RW	3'b0
40.0.11	SWREF	Select LDO Reference 0: (Default) 1: Change LDO reference to local	RW	1'h0
40.0.10	sel_low_freq	PHY Clock Select 0: phy_xtalclk = 25 MHz from crystal (Default) 1: phy_xtalclk = clk from slow osc	RW	1'h0
40.0.9:0	Reserved	Reserved	RW	10'b0
Register 23h (36) – EDPD Control Register				
36.15:6	Reserved	Reserved	R	10'h000
36.5:4	Reserved	Reserved	RW	2'b00
36.3:2	Reserved	Reserved	RW	2'b00
36.1	Reserved	Reserved	RW	1'b0
36.0	EDPD_Enable	Energy Detect Power Down Enable 0: EDPD is not enabled 1: EDPD is enabled	RW	1'b0

Note:

2. RW = Read/Write.
   RC = Read-cleared
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.

Absolute Maximum Ratings[1]

Supply Voltage
(DVDDL, AVDDL, AVDDL_PLL)..... -0.5V to V_{DD}+10%
(AVDDH)..... -0.5V to V_{DD} +10%
(DVDDH)..... -0.5V to V_{DD} (3.3V)+10%
Input Voltage (all inputs) ..... -0.5V to V_{DD} +10%
Output Voltage (all outputs) ..... -0.5V to V_{DD} +10%
Lead Temperature (soldering, 10sec.)..... 260°C
Storage Temperature (T_s) .....-55°C to +150°C

Operating Ratings[2]

Supply Voltage
(DVDDL, AVDDL, AVDDL_PLL).... +1.140V to +1.260V
(AVDDH)..... +3.135V to +3.465V
(DVDDH @ 3.3V) ..... +3.135V to +3.465V
(DVDDH @ 2.5V) ..... +2.375V to +2.625V
(DVDDH @ 1.8V) ..... +1.710V to +1.890V
Ambient Temperature
(T_A Commercial: KSZ9031RNXC)..... 0°C to +70°C
(T_A Industrial: KSZ9031RNXI) .....-40°C to +85°C
Maximum Junction Temperature (T_J Max)..... 125°C
Thermal Resistance (θ_{JA}).....31.85°C/W
Thermal Resistance (θ_{JC}).....8.07°C/W

Electrical Characteristics[3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current – Core / Digital I/Os						
I_{CORE}	1.2V total of: DVDDL (digital core) + AVDDL (analog core) + AVDDL_PLL (PLL)	1000Base-T Link-up (no traffic)		210		mA
		1000Base-T Full-duplex @ 100% utilization		222		mA
		100Base-TX Link-up (no traffic)		61.8		mA
		100Base-TX Full-duplex @ 100% utilization		62.1		mA
		10Base-T Link-up (no traffic)		6.8		mA
		10Base-T Full-duplex @ 100% utilization		7.3		mA
		Power Saving Mode (cable unplugged)		TBD		mA
		Software Power Down Mode (Reg. 0h.11 =1)		1.1		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		TBD		mA
$I_{DVDDH\_1.8}$	1.8V for digital I/Os (RGMII operating @ 1.8V)	1000Base-T Link-up (no traffic)		11.2		mA
		1000Base-T Full-duplex @ 100% utilization		23.5		mA
		100Base-TX Link-up (no traffic)		8.3		mA
		100Base-TX Full-duplex @ 100% utilization		9.6		mA
		10Base-T Link-up (no traffic)		5.8		mA
		10Base-T Full-duplex @ 100% utilization		6.0		mA
		Power Saving Mode (cable unplugged)		TBD		mA
		Software Power Down Mode (Reg. 0h.11 =1)		4.6		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		TBD		mA
$I_{DVDDH\_2.5}$	2.5V for digital I/Os (RGMII operating @ 2.5V)	1000Base-T Link-up (no traffic)		14.7		mA
		1000Base-T Full-duplex @ 100% utilization		31.0		mA
		100Base-TX Link-up (no traffic)		11.1		mA
		100Base-TX Full-duplex @ 100% utilization		12.9		mA
		10Base-T Link-up (no traffic)		7.9		mA
		10Base-T Full-duplex @ 100% utilization		8.1		mA
		Power Saving Mode (cable unplugged)		TBD		mA
		Software Power Down Mode (Reg. 0h.11 =1)		6.7		mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		TBD		mA
$I_{DVDDH\_3.3}$	3.3V for digital I/Os (RGMII operating @ 3.3V)	1000Base-T Link-up (no traffic)		22.0		mA
		1000Base-T Full-duplex @ 100% utilization		42.4		mA
		100Base-TX Link-up (no traffic)		15.4		mA
		100Base-TX Full-duplex @ 100% utilization		17.5		mA
		10Base-T Link-up (no traffic)		10.9		mA
		10Base-T Full-duplex @ 100% utilization		11.0		mA
		Power Saving Mode (cable unplugged)		TBD		mA
		Software Power Down Mode (Reg. 0h.11 =1)		10.6		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		TBD		mA
Supply Current – Transceiver (equivalent to current draw through external transformer center taps for PHY transceivers with current-mode transmit drivers)						
$I_{AVDDH\_2.5}$	2.5V for transceiver	1000Base-T Link-up (no traffic)		56.4		mA
		1000Base-T Full-duplex @ 100% utilization		55.4		mA
		100Base-TX Link-up (no traffic)		23.2		mA
		100Base-TX Full-duplex @ 100% utilization		23.2		mA
		10Base-T Link-up (no traffic)		10.0		mA
		10Base-T Full-duplex @ 100% utilization		21.5		mA
		Power Saving Mode (cable unplugged)		TBD		mA
		Software Power Down Mode (Reg. h0.11 =1)		2.1		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		TBD		mA
$I_{AVDDH\_3.3}$	3.3V for transceiver	1000Base-T Link-up (no traffic)		64.7		mA
		1000Base-T Full-duplex @ 100% utilization		63.7		mA
		100Base-TX Link-up (no traffic)		27.3		mA
		100Base-TX Full-duplex @ 100% utilization		27.3		mA
		10Base-T Link-up (no traffic)		14.2		mA
		10Base-T Full-duplex @ 100% utilization		24.8		mA
		Power Saving Mode (cable unplugged)		TBD		mA
		Software Power Down Mode (Reg. h0.11 =1)		3.4		mA
		Chip Power Down Mode (strap-in pins MODE[3:0] = “0111”)		TBD		mA
CMOS Inputs						
V_{IH}	Input High Voltage	DVDDH = 3.3V	2.0			V
		DVDDH = 2.5V	1.8			V
		DVDDH = 1.8V	TBD			V
V_{IL}	Input Low Voltage	DVDDH = 3.3V			0.8	V
		DVDDH = 2.5V			0.7	V
		DVDDH = 1.8V			TBD	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DDIO}		-10	10	µA

Symbol	Parameter	Condition	Min	Typ	Max	Units
CMOS Outputs						
V_{OH}	Output High Voltage	DVDDH = 3.3V	2.4			V
		DVDDH = 2.5V	2.0			V
		DVDDH = 1.8V	TBD			V
V_{OL}	Output Low Voltage	DVDDH = 3.3V			0.4	V
		DVDDH = 2.5V			0.4	V
		DVDDH = 1.8V			TBD	V
$\|I_{oz}\|$	Output Tri-State Leakage				10	µA
LED Outputs						
I_{LED}	Output Drive Current	Each LED pin (LED1, LED2)		8		mA
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				± 0.25	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of I_{SET}	$R(I_{SET})$ = 12.1K		0.535		V
	Output Jitter	Peak-to-peak		0.7		ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
	Harmonic Rejection	Transmit all-one signal sequence		-31		dB
10Base-T Receive						
V_{SQ}	Squelch Threshold	5 MHz square wave	300	400		mV

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. T_A = 25°C. Specification is for packaged product only.

Timing Diagrams

RGMII Timing

The KSZ9031RNX RGMII timing conforms to the timing requirements per the RGMII Version 2.0 Specification.

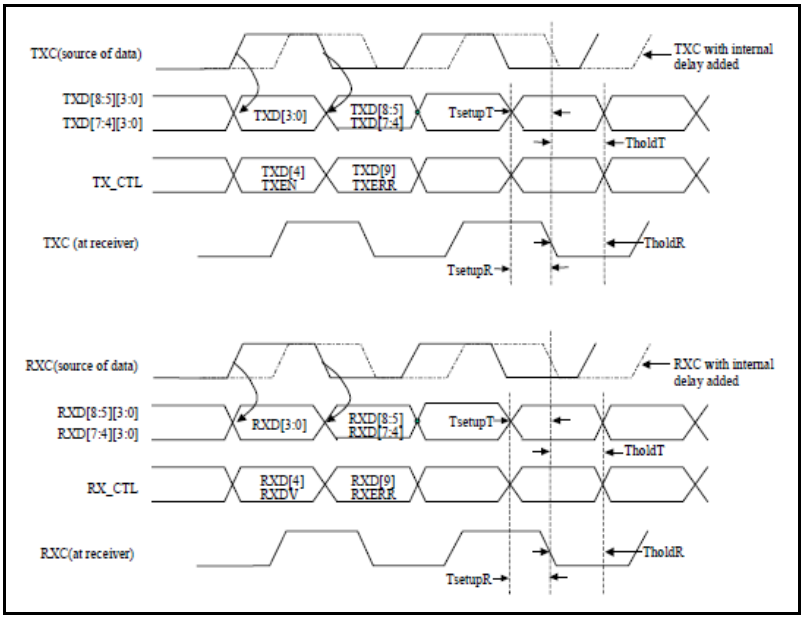


Figure 8. RGMII v2.0 Specification (Figure 3 – Multiplexing and Timing Diagram)

Timing Parameter	Description	Min	Typ	Max	Unit
TskewT	Data to Clock output Skew (at Transmitter)	-500		500	ps
TskewR	Data to Clock input Skew (at Receiver)	1		2.6	ns
Tcyc (1000Base-T)	Clock Cycle Duration for 1000Base-T	7.2	8	8.8	ns
Tcyc (100Base-TX)	Clock Cycle Duration for 100Base-TX	36	40	44	ns
Tcyc (10Base-T)	Clock Cycle Duration for 10Base-T	360	400	440	ns

Table 11. RGMII v2.0 Specification (Timing Specifics from Table 2)

Auto-Negotiation Timing

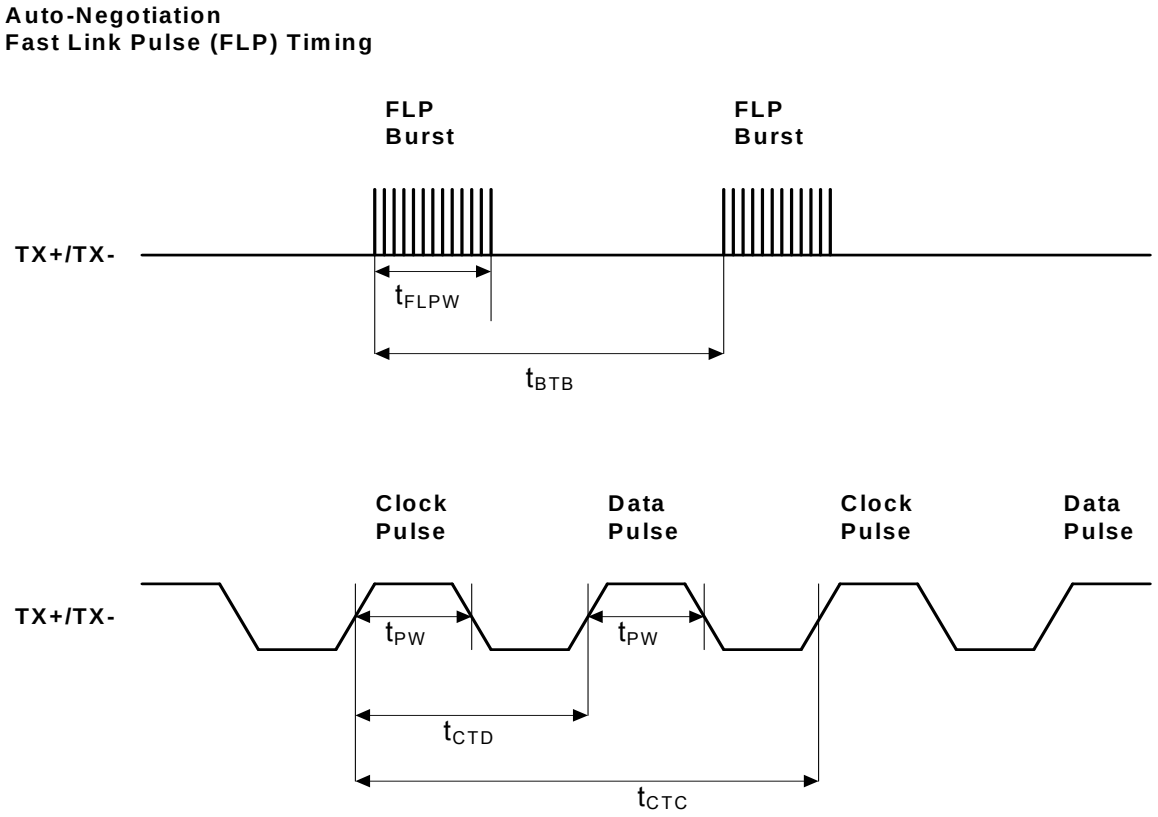


Figure 9. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst width		2		ms
t_{PW}	Clock/Data Pulse width		100		ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
	Number of Clock/Data Pulse per FLP Burst	17		33	

Table 12. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

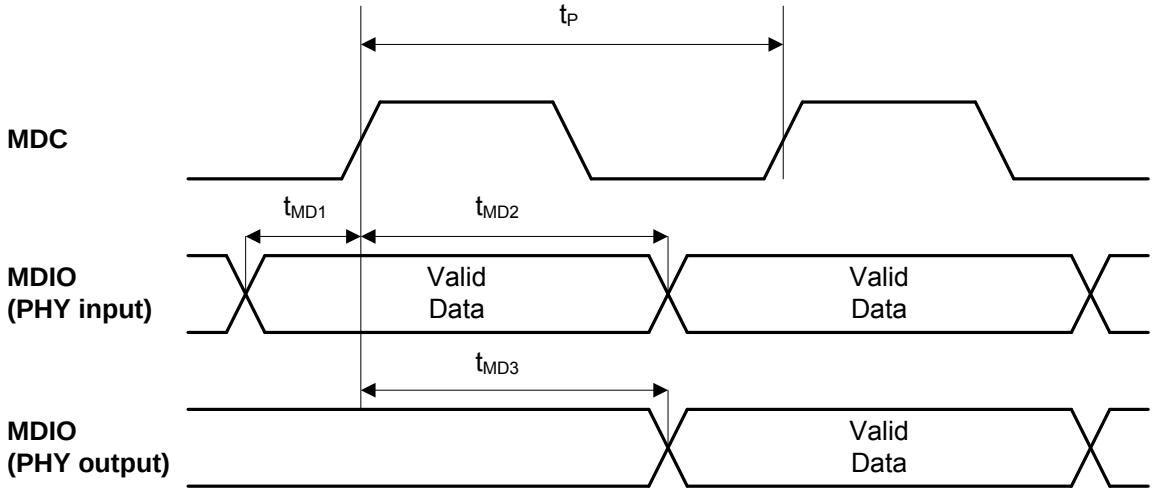


Figure 10. MDC/MDIO Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	MDC period		400		ns
t_{1MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	10			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	0			ns

Table 13. MDC/MDIO Timing Parameters

Reset Timing

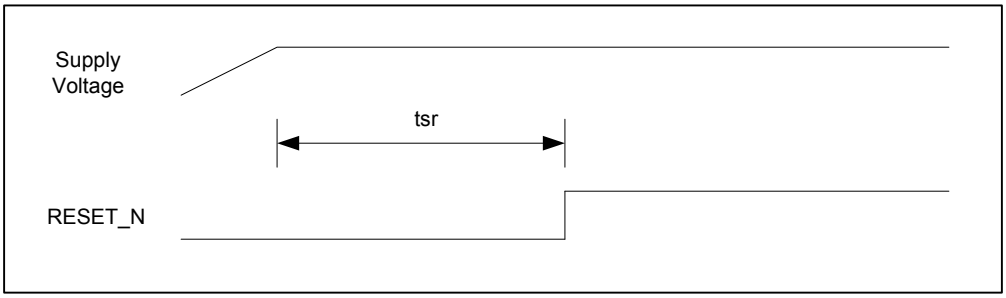


Figure 11. Reset Timing

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltage to reset high	10		ms

Table 14. Reset Timing Parameters

The recommended power sequence is to have the transceiver (AVDDH) and VDDI/O (DVDDH) power rails come up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL). If this is not possible, then reduce the 1.2V core to transceiver and VDDI/O power-up delay to <200us.

There is no power sequence requirement between transceiver (AVDDH) and VDDI/O (DVDDH) power rails.

All supply voltages' power-up waveforms should be monotonic.

After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) Interface.

Reset Circuit

The following reset circuit is recommended for powering up the KSZ9031RNX if reset is triggered by the power supply.

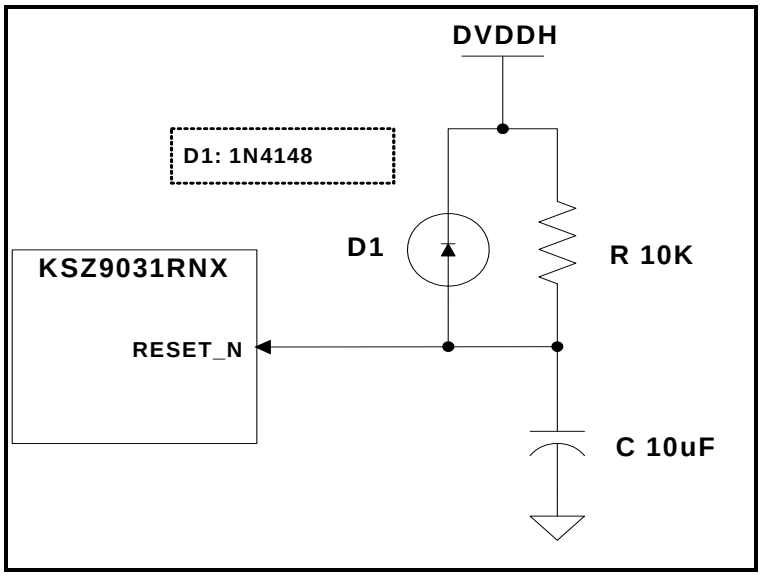


Figure 12. Recommended Reset Circuit

The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ9031RNX device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

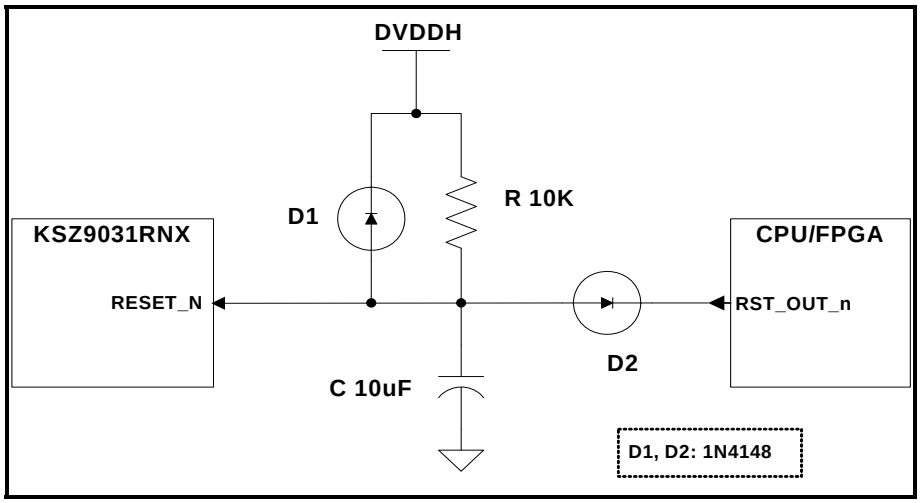


Figure 13. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output

Reference Circuits – LED Strap-in Pins

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in the following figure for 3.3V and 2.5V DVDDH.

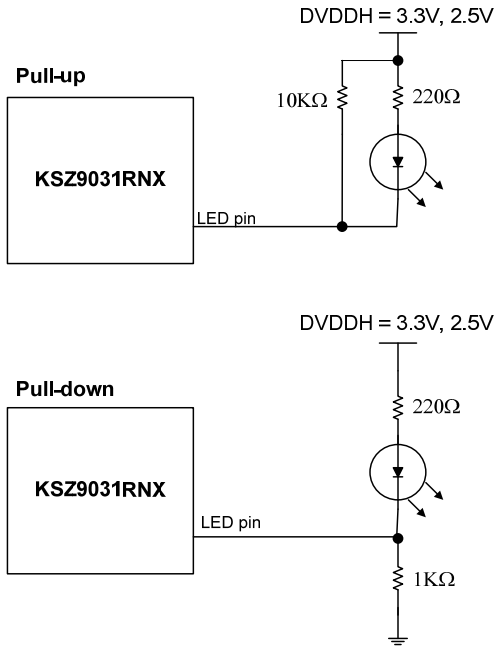


Figure 14. Reference Circuits for LED Strapping Pins

For 1.8V DVDDH, LED indication support is not recommended due to the low voltage. Without the LED indicator, the PHYAD1 and PHYAD0 strapping pins are functional with 10K pull-up to 1.8V DVDDH for a value of ‘1’, and with 1.0K pull-down to ground for a value of ‘0’.

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ9031RNX. The reference clock is 25 MHz for all operating modes of the KSZ9031RNX.

The following figure and table shows the reference clock connection to pins XI and XO of the KSZ9031RNX, and the reference clock selection criteria.

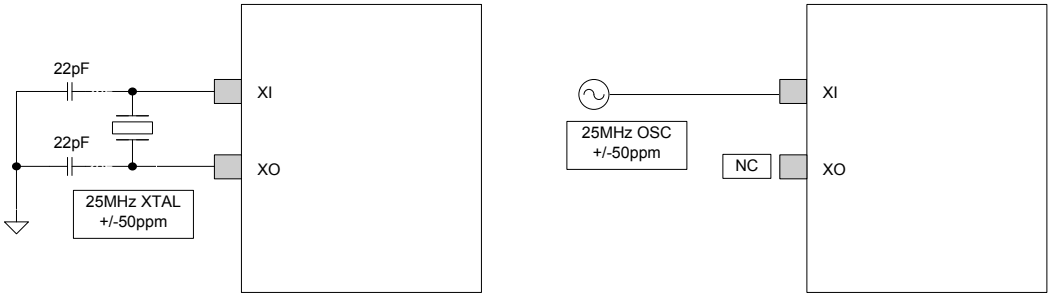


Figure 15. 25 MHz Crystal / Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm

Table 15. Reference Crystal/Clock Selection Criteria

Magnetics Specification

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements.

The following tables provide recommended magnetic characteristics and a list of qualified magnetics for the KSZ9031RNX.

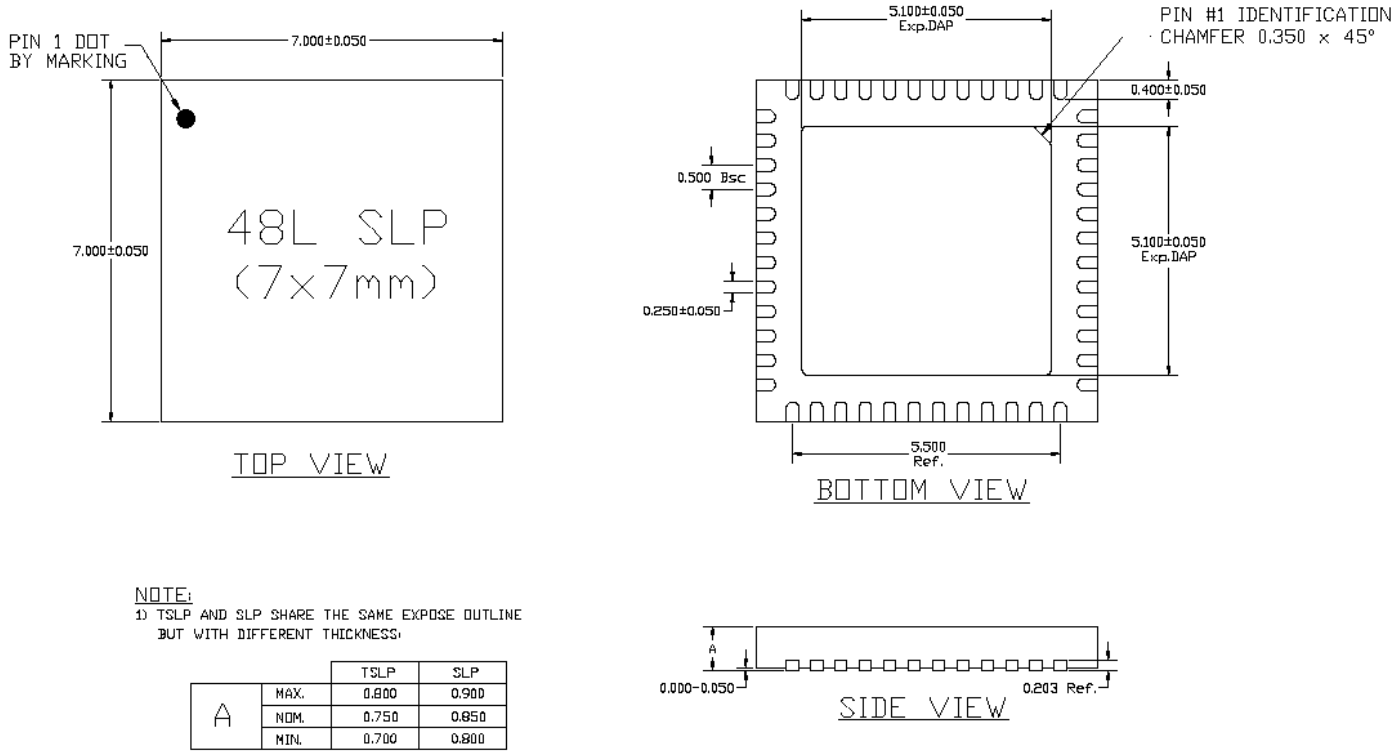
Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350μH	100mV, 100kHz, 8mA
Insertion loss (max.)	1.0dB	0MHz – 100MHz
HIPOT (min.)	1500Vrms	

Table 16. Magnetics Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Pulse	H5007NL	Yes	1
TDK	TLA-7T101LF	Yes	1

Table 17. Qualified Single Port 10/100/1000 Magnetics

Package Information



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

48-Pin (7mm x 7mm) QFN

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