PC/104-Plus Specification

Version 1.2

August 2001

Please Note

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REVISION HISTORY

Draft 0.7, November 20, 1996 - Preliminary Draft
a. Formatted to meet the requirements of the PC/104 Consortium.
b. Modify the component restrictions across and to each side of the PC/104 connectors (three sides, .400" from each edge, 4.35" top clearance, .100" bottom clearance).

Draft 0.8, December 16, 1996 - Cleanup for Release
a. Correct general typos.
b. Correct word reference error.
c. Add QuickSwitch part number and clarify Mux requirements.
d. Change PCI ONLY to PCI-Only and add note.
e. Correct figure 4 and Figure 5 errors.
f. Correct typo in Table 3.

Draft 0.9, January 10, 1997 - Cleanup for Release
a. Cleanup minor grammatical errors.

Version 1.0, February 1997 - Initial Release
a. Grammatical changes and cleanup per review recommendations.
b. Change Footnote 1 on Page 2 to show future support for the M66EN (66MHz Enable) signal.
c. Add signals PRSNT[1:2]* and CLKRUN* to Figure 1 to encompass all unused PCI signals.
d. Moved the Mechanical section after the Electrical section.
e. Clarified the KEY pin usage for universal modules and defined them as ground connections.
f. Clarified pin 1 for the PC/104-Plus connectors on Figure 4.
g. Added an example manufacturer and part No. for the PCI connector (Figure 5) and Shroud (Figure 6).
h. Modified Figure 2, Table 1, and some text under Section 2.2 to add routing recommendations for the PCI interrupt lines INTA - INTD.

Version 1.1, June 1997 - Minor Editorial Corrections
a. Correct errors in the Table of Figures and Table of Tables.
b. Correct dimensions on the PCI connector (Figure 5).
c. Correct part number and dimensions on the shroud (Figure 6).
d. Correct general typos and update reference information.

Version 1.2, April 2001
a. Added PCI Connector Specifications and PCI-104 name for “PCI Only”.
b. Added PC/104 8-Bit and 16-Bit Connector Specification.
c. Removed specific company references.
d. Corrected PCISIG and consortium addresses and phone numbers.
# TABLE OF CONTENTS

1. INTRODUCTION ............................................................................................................................................. 1
   1.1 SUMMARY OF KEY DIFFERENCES FROM PC/104 SPECIFICATION: ................................................. 1
   1.2 SUMMARY OF KEY DIFFERENCES (120-pin PCI and PCI Local Bus Specification) ............... 1
   1.3 REFERENCES ............................................................................................................................................. 1

2. PCI SIGNAL DEFINITION .............................................................................................................................. 2
   2.1 PCI BUS SIGNAL DESCRIPTION .............................................................................................................. 3
      2.1.1 Address and Data .......................................................................................................................... 3
      2.1.2 Interface Control Pins .................................................................................................................. 3
      2.1.3 Error Reporting ........................................................................................................................... 3
      2.1.4 Arbitration (Bus Masters Only) .................................................................................................... 3
      2.1.5 System ............................................................................................................................................ 3
      2.1.6 Interrupts ....................................................................................................................................... 3
   2.2 SIGNAL GROUPING ................................................................................................................................... 4

3. ELECTRICAL SPECIFICATION ..................................................................................................................... 5
   3.1 PC/104 BUS .............................................................................................................................................. 5
   3.2 PCI BUS .................................................................................................................................................. 5
      3.2.1 Signal Definitions ......................................................................................................................... 5
      3.2.2 Signal Assignments .................................................................................................................... 5
      3.2.3 Power and Ground Pins ............................................................................................................. 5
      3.2.4 Key Locations .............................................................................................................................. 5
      3.2.5 AC/DC Signal Specifications ..................................................................................................... 5
   3.3 MODULE POWER REQUIREMENTS ..................................................................................................... 6

4. LEVELS OF CONFORMANCE .......................................................................................................................... 6
   4.1 PC/104-PLUS "COMPLIANT" ............................................................................................................. 6
   4.2 PC/104-PLUS "BUS-COMPATIBLE" ............................................................................................... 6
   4.3 PCI-104 .................................................................................................................................................. 6

5. MECHANICAL SPECIFICATION ..................................................................................................................... 7
   5.1 MODULE DIMENSIONS ..................................................................................................................... 7
   5.2 CONNECTOR AND SHROUD ............................................................................................................. 7

6. TYPICAL MODULE STACK .......................................................................................................................... 8

APPENDICES
A. MECHANICAL DIMENSIONS ...................................................................................................................... A-1
B. BUS SIGNAL ASSIGNMENTS .................................................................................................................. B-1
TABLE OF FIGURES

FIGURE 1: PCI Pin List .......................................................................................................................... 2
FIGURE 2: Signal Select .......................................................................................................................... 4
FIGURE 3: Typical Module Stack .......................................................................................................... 8
FIGURE 4: Module Dimensions ............................................................................................................ A-2
FIGURE 5: PC/104-Plus and PCI-104 PCI Connector ........................................................................ A-3
FIGURE 6: PCI Shroud .......................................................................................................................... A-3
FIGURE 7: PC/104-Plus and PCI-104 PCI Connector Specifications ............................................... A-4
FIGURE 8: PC/104 8-Bit and 16-Bit ISA Connector Specification ................................................ A-5

TABLE OF TABLES

TABLE 1: Rotary Switch Settings ......................................................................................................... 4
TABLE 2: Module Power Requirements .............................................................................................. 6
TABLE 3: PC/104-Plus Bus Signal Assignments ............................................................................... B-2
TABLE 4: PC/104 Bus (Reference Only) ............................................................................................ B-3
1. INTRODUCTION

While the PC/AT architecture is becoming increasingly popular in embedded applications, there is an increasing need for a higher performance Bus throughput. This is especially true when it comes to graphics devices as well as other high speed I/O devices such as networks.

This document supplies the mechanical and electrical specifications for the “PC/104-Plus” and incorporates all of the PC/104 features, with the added advantage of the high speed PCI bus. The physical size, mounting configuration and electrical interconnect portion of the PC/104 specification shall remain unchanged.

1.1 Summary of Key Differences From PC/104 Specification:

- A third connector opposite the PC/104 connectors supports the PCI bus.
- Changes to the component height requirements increase the flexibility of the module.
- Control logic added to handle the requirements for the high speed bus.

1.2 Summary of Key Differences (120-pin PCI and PCI Local Bus Specification)

- The PCI bus connector is a 4x30 (120-pin) 2mm pitch stackthrough connector as opposed to the 124-pin edge connector on standard 32-bit PCI Local Bus.
- The 120-pin PCI does not support 64-bit Extensions, JTAG, PRSNT, or CLKRUN signals.

1.3 References

This document covers the addition of the PCI functions. The following documents should be used as reference for a detailed understanding of the overall system requirements:

- PC/104 Specification -- Version 2.4
- PCI Local Bus Specification -- Revision 2.1

Contact the PCI Special Interest Group office for the latest revision of the PCI specification:

PCI Special Interest Group
5440 SW Westgate Drive, Suite 217
Portland, OR 97221
800.433.5177 (U.S.)  503.291.2569 (International)

If errors are found in this document, please send a written copy of the suggested corrections to:

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2. PCI SIGNAL DEFINITION

Figure 1 shows the pins in functional groups, with the required pins on the left and the optional pins on the right side. The shaded pins on the right are unsupported features, but are included to show the entire PCI bus as defined in the PCI Revision 2.1 Specification. This version of the PCI bus is intended as a 32-bit bus running at 33MHz and therefore, 64-bit extension and 66MHz\(^1\) are not supported at this time. Also not supported are the boundary scan features (JTAG), Present (PRSRT[1:2]*), and Clock running (CLKRUN*). The direction indication on the pins assumes a combination master/target device.

\(^1\) The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. To support future enhancements, the M66EN signal should be grounded on any module that cannot support 66MHz and left open for modules that can support a 66MHz clock.
2.1 PCI Bus Signal Description

2.1.1 Address and Data

AD[31:00]  Address and Data are multiplexed. A bus transaction consists of an address cycle followed by one or more data cycles.

C/BE[3:0]*  Bus Command/Byte Enables are multiplexed. During the address cycle, the command is defined. During the Data cycle, they define the byte enables.

PAR  Parity is even on AD[31:00] and C/BE[3:0]* and is required.

2.1.2 Interface Control Pins

FRAME*  Frame is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.

TRDY*  Target Ready indicates the selected devices ability to complete the current data cycle of the transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle.

IRDY*  Initiator Ready indicates the master's ability to complete the current data cycle of the transaction.

STOP*  Stop indicates the current selected device is requesting the master to stop the current transaction.

DEVSEL*  Device Select is driven by the target device when its address is decoded.

IDSEL  Initialization Device Select is used as a chip-select during configuration.

LOCK*  Lock indicates an operation that may require multiple transactions to complete.

2.1.3 Error Reporting

PERR*  Parity Error is for reporting data parity errors.

SERR*  System Error is for reporting address parity errors.

2.1.4 Arbitration (Bus Masters Only)

REQ*  Request indicates to the arbitrator that this device desires use of the bus.

GNT*  Grant indicates to the requesting device that access has been granted.

2.1.5 System

CLK  Clock provides timing for all transactions on the PCI bus.

RST*  Reset is used to bring PCI-specific registers to a known state.

2.1.6 Interrupts

INTA*  Interrupt A is used to request Interrupts.

INTB*  Interrupt B is used to request Interrupts only for multi-function devices.

INTC*  Interrupt C is used to request Interrupts only for multi-function devices.

INTD*  Interrupt D is used to request Interrupts only for multi-function devices.
2.2 Signal Grouping

A means of selecting the appropriate signals must be established that will easily allow for the installation and configuration of add-in PC/104-Plus modules. Figure 2 shows such a method:

Figure 2: Signal Select

The multiplexer chips are Dual 4:1 Mux/Demux chips. They provide a 5Ω switch that connects the input and output together. These switches provide a bi-directional path with no signal propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. This is typically 250ps at 50pF Load.

Other methods of configuring the modules are possible, but the rotary switch is the most convenient, cleanest and provides for the least possible error in configuration.

The clocks are tuned on the Host Board such that the length of CLK3 trace is ≈0.662" less than CLK2, CLK2 trace is ≈0.662" less than CLK1, and CLK1 trace is ≈0.662" less than CLK0. Therefore, the first module on the stack must select CLK0 (the longest trace), the second CLK1, etc. This provides basically no clock skew between modules. Table 1 shows the appropriate switch setting and signals used for each module in the stack. It is recommended that additional Mux chips be added to route Interrupts if required. Use one Mux for 1 to 2 Interrupts or two Mux’s for 3 to 4 Interrupts.

Table 1: Rotary Switch Settings

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>Module Slot</th>
<th>REQ*</th>
<th>GNT*</th>
<th>CLK</th>
<th>ID Address</th>
<th>INT0*</th>
<th>INT1*</th>
<th>INT2*</th>
<th>INT3*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 or 4</td>
<td>1</td>
<td>REQ0*</td>
<td>GNT0*</td>
<td>CLK0</td>
<td>AD20</td>
<td>INTA*</td>
<td>INTB*</td>
<td>INTC*</td>
<td>INTD*</td>
</tr>
<tr>
<td>1 or 5</td>
<td>2</td>
<td>REQ1*</td>
<td>GNT1*</td>
<td>CLK1</td>
<td>AD21</td>
<td>INTA*</td>
<td>INTB*</td>
<td>INTC*</td>
<td>INTD*</td>
</tr>
<tr>
<td>2 or 6</td>
<td>3</td>
<td>REQ2*</td>
<td>GNT2*</td>
<td>CLK2</td>
<td>AD22</td>
<td>INTA*</td>
<td>INTB*</td>
<td>INTC*</td>
<td>INTD*</td>
</tr>
<tr>
<td>3 or 7</td>
<td>4</td>
<td>REQ2*</td>
<td>GNT2*</td>
<td>CLK3</td>
<td>AD23</td>
<td>INTA*</td>
<td>INTB*</td>
<td>INTC*</td>
<td>INTD*</td>
</tr>
</tbody>
</table>

Note 1: Because module slots 3 and 4 share REQ2/GNT2, they cannot both be bus master devices.
3. ELECTRICAL SPECIFICATION

3.1 PC/104 Bus

The electrical specifications for the PC/104 bus for bus drive current, bus termination, pullup/pulldown resistors, etc. are unchanged and are defined in the PC/104 Specification. The signal assignments for the J1/P1 and J2/P2 connector are given in Appendix B, Table 4: PC/104 Bus (Reference Only).

3.2 PCI Bus

The PCI Bus mechanical interface is a stackable 30x4 header. This interface carries all of the required PCI signals per PCI Local Bus Specification Version 2.1.

3.2.1 Signal Definitions

For full details on the electrical requirements for the PCI bus, reference the PCI Local Bus Specification Version 2.1.

3.2.2 Signal Assignments

Signals are assigned in the same relative order as in the PCI Local Bus Specification, but transformed to the corresponding header connector pins. Because of the stackthrough nature of the bus, slot-specific signals are duplicated for each plug-in module. The system has been designed to accommodate 4 PC/104-Plus modules, so multiple sets of the signals have been duplicated to accommodate one signal for each module. These four signal groups include: IDSEL[3:0] - CLK[3:0] - REQ*[2:0] - GNT*[2:0]. Signal assignments for the J3/P3 connector are given in Appendix B, Table 3: PC/104-Plus Bus Signal Assignments.

3.2.3 Power and Ground Pins

The total number of power and ground signals remains the same, but the +3.3 V pins have been reduced by two and the ground pins have been increased by two. The change was the result of signal grouping on the bus and has no effect on performance or integrity.

3.2.4 Key Locations

The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. Universal boards which can support either signal levels will have both key pins implemented. Universal boards must therefore be located at the top of the stack. See Appendix B, Table 3: PC/104-Plus Bus Signal Assignments.

3.2.5 AC/DC Signal Specifications

All bus timing and signal levels are identical to the PCI Local Bus Specification Revision 2.1.
3.3 Module Power Requirements

Table 2 specifies the voltage and maximum power requirements for each PC/104-Plus module. It should be noted that although the maximum requirements as specified are the same as the standard PC/104 Specification, care should be used in designing PC/104-Plus modules to guarantee the least possible power consumption. A worst case module as specified could use almost 39 Watts of power, which would basically be unacceptable in most systems.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3V¹</td>
<td>3.00</td>
<td>3.60</td>
<td>3A</td>
<td>10.8 W</td>
</tr>
<tr>
<td>+5V</td>
<td>4.75</td>
<td>5.25</td>
<td>2A</td>
<td>10.5 W</td>
</tr>
<tr>
<td>+12V</td>
<td>11.4</td>
<td>12.6</td>
<td>1A</td>
<td>12.6 W</td>
</tr>
<tr>
<td>-5V</td>
<td>-5.25</td>
<td>-4.75</td>
<td>0.2A</td>
<td>1.05 W</td>
</tr>
<tr>
<td>-12V</td>
<td>-12.6</td>
<td>-11.4</td>
<td>0.3A</td>
<td>3.78 W</td>
</tr>
</tbody>
</table>

Note 1: Host Boards implementing “5 volt PCI signaling” are not required to supply 3.3 volts to the modules, but must provide a bus and decoupling. If 3.3 volts is required for a module using the “5 volt PCI signaling” method, provisions should be made to provide its own 3.3 volts by means of an onboard regulator or some other input source. Host Boards implementing “3.3 volt PCI signaling” are required to supply 3.3 volts to the modules.

4. LEVELS OF CONFORMANCE

This section provides terminology intended to assist manufacturers and users of PC/104-Plus bus-compatible products in defining and specifying conformance with the PC/104-Plus Specification.

4.1 PC/104-Plus "Compliant"

This refers to "PC/104-Plus form-factor" devices that conform to all non-optional aspects of the PC/104-Plus Specification, including both mechanical and electrical specifications.

4.2 PC/104-Plus "Bus-compatible"

This refers to devices which are not "PC/104-Plus form-factor" (i.e., do not comply with the module dimensions of the PC/104-Plus Specification), but provide male or female PC/104-Plus bus connectors that meets both the mechanical and electrical specifications provided for the PC/104-Plus bus connectors.

4.3 PCI-104

Because the PC/104-Plus standard encompasses two different buses (i.e. PC/104 104-pin "ISA" bus and 120-pin "PCI" bus), it is possible for PC/104-Plus modules to implement only the PCI bus. Such modules shall have the designation "PCI-104". For example: PCI-104 "Compliant" or PCI-104 "Bus-compatible". This option precludes stacking standard PC/104 Modules.
5. MECHANICAL SPECIFICATION

5.1 Module Dimensions

The mechanical dimensions for this module are identical to PC/104 Specification with the exception of the added connector (J3), some modifications to the I/O connector area, and changes to the component height restrictions. The component height on the top side has been reduced from 0.435" to 0.345" and the bottom has been increased from 0.100" to 0.190". The component restrictions across and to each side of the PC/104 connectors (three sides, 0.400" from each edge) remains the same as the PC/104 Specification. The mechanical dimensions and restrictions are given in Appendix A, Figure 4: Module Dimensions.

5.2 Connector and Shroud

The PC/104-Plus connector for the PCI bus is a 4x30 (120-pin) 2mm pitch connector. The shroud should be installed on the bottom of the PC board when a stackthrough connector is used. The mechanical dimensions and restrictions are given in Appendix A, Figure 5: PC/104-Plus and PCI-104 PCI Connector.
6. TYPICAL MODULE STACK

Figure 3 shows a typical module stack with 2 PC/104-Plus modules, 1 PC/104 16-Bit module, and 1 PC/104 8-Bit module. The maximum configuration for the PCI bus of PC/104-Plus modules is 4 plus the Host Board. If standard PC/104 modules are used in the stack, they must be the top module(s) because they will normally not include the PCI bus.
APPENDIX A

MECHANICAL DIMENSIONS
Recommended Keep Out Area For Extractor
Top (Horizontal Stripe)
Bottom (Both Strips)
Both Edges

I/O Connectors may overhang in this area
(Includes Mating Connector)

Install Switch as close as possible to the signal source.

Unshaded Area
Top Clearance = .345
Bottom Clearance = .190

Shaded Area (3 Sides)
Top Clearance = .435
Bottom Clearance = .100

Max Component Height = .345
Connector Shroud
Max Component Height = .190
PC/104-Plus

Figure 5: PC/104-Plus and PCI-104 PCI Connector

Figure 6: PCI Shroud

NOTE:

LOCKING PIECES ARE NOT REQUIRED IF THE SHROUD IS A PRESS FIT ONTO THE LONG CONNECTOR PINS OR OTHERWISE SECURED.
Figure 7: PC/104-Plus and PCI-104 PCI Connector Specifications

**MATERIALS**

**HOUSING:** HIGH TEMP THERMOPLASTIC, UL RATED 94-V0  
**CONTACT:** PHOSPHOR BRONZE  
**SOLDER:** TIN-LEAD (63-37), IF APPLICABLE  
**SOLDER CLIP:** ALUMINUM ALLOY, IF APPLICABLE

**CONTACT FINISH**

**FEMALE INTERFACE:** 20 MICROINCHES MINIMUM HARD GOLD  
**MALE INTERFACE:** GOLD FLASH MINIMUM  
**SOLDER TAIL:** 100 MICROINCHES MINIMUM SOLDER  
**UNDERPLATE:** 50 MICROINCHES MINIMUM NICKEL

**MECHANICAL PERFORMANCE**

**INSERTION FORCE:** 2.5 OUNCE PER PIN MAXIMUM  
**WITHDRAW FORCE:** 1 OUNCE MINIMUM AVERAGE  
**NORMAL FORCE:** 50 GRAMS MINIMUM (PER BEAM)  
**DURABILITY:** 50 CYCLES MINIMUM  
**OPERATING TEMP:** -55° C TO +85° C

**ELECTRICAL PERFORMANCE**

**CONTACT RESISTANCE:** <30 MILLIOHMS MAXIMUM  
**CURRENT CAPACITY:** 1 AMP CONTINUOUS PER PIN  
**DIELECTRIC STRENGTH:** 500 VAC  
**INSULATION RESISTANCE:** 5,000 MEGOHMS MINIMUM
Figure 8: PC/104 8-Bit and 16-Bit ISA Connector Specification

NOTES:

1. PRESS FIT COMPLIANT PINS PER DIN 41612 PART 5 AND IEC 352-5 CAN BE USED INSTEAD OF SQUARE PINS AS SHOWN.
2. CONFIGURATION CAN BE MADE OF ONE OR MORE PIECES.
MATERIALS
HOUSING: HIGH TEMP THERMOPLASTIC, UL RATED 94-V0
CONTACT: PHOSPHOR BRONZE
SOLDER: TIN-LEAD (63-37), IF APPLICABLE
SOLDER CLIP: ALUMINUM ALLOY, IF APPLICABLE

CONTACT FINISH
FEMALE INTERFACE: 20 MICROINCHES MINIMUM HARD GOLD
MALE INTERFACE: GOLD FLASH MINIMUM
SOLDER TAIL: 100 MICROINCHES MINIMUM SOLDER
UNDERPLATE: 50 MICROINCHES MINIMUM NICKEL

MECHANICAL PERFORMANCE
INSERTION FORCE: 3.5 OUNCE PER PIN MAXIMUM
WITHDRAW FORCE: 1 OUNCE MINIMUM AVERAGE
NORMAL FORCE: 50 GRAMS MINIMUM (PER BEAM)
DURABILITY: 50 CYCLES MINIMUM
OPERATING TEMP: -55° C TO +85° C

ELECTRICAL PERFORMANCE
CONTACT RESISTANCE: <30 MILLIOHMS MAXIMUM
CURRENT CAPACITY: 1 AMP CONTINUOUS PER PIN
DIELECTRIC STRENGTH: 1000 VAC
INSULATION RESISTANCE: 5,000 MEGOHMS MINIMUM
APPENDIX B

BUS SIGNAL ASSIGNMENTS
### Table 3: PC/104-Plus Bus Signal Assignments

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND/5.0V KEY ²</td>
<td>Reserved</td>
<td>+5</td>
<td>AD00</td>
</tr>
<tr>
<td>2</td>
<td>VI/O</td>
<td>AD02</td>
<td>AD01</td>
<td>+5V</td>
</tr>
<tr>
<td>3</td>
<td>AD05</td>
<td>AD07</td>
<td>GND</td>
<td>AD06</td>
</tr>
<tr>
<td>4</td>
<td>C/BE0*</td>
<td>AD04</td>
<td>AD03</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>AD09</td>
<td>AD08</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>AD11</td>
<td>VI/O</td>
<td>AD10</td>
<td>M66EN</td>
</tr>
<tr>
<td>7</td>
<td>AD14</td>
<td>AD13</td>
<td>GND</td>
<td>AD12</td>
</tr>
<tr>
<td>8</td>
<td>+3.3V</td>
<td>C/BE1*</td>
<td>AD15</td>
<td>+3.3V</td>
</tr>
<tr>
<td>9</td>
<td>SERR*</td>
<td>GND</td>
<td>SB0*</td>
<td>PAR</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>PERR*</td>
<td>+3.3V</td>
<td>SDONE</td>
</tr>
<tr>
<td>11</td>
<td>STOP*</td>
<td>+3.3V</td>
<td>LOCK*</td>
<td>GND</td>
</tr>
<tr>
<td>12</td>
<td>+3.3V</td>
<td>TRDY*</td>
<td>GND</td>
<td>DEVSEL*</td>
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<td>GND</td>
<td>IRDY*</td>
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<td>14</td>
<td>GND</td>
<td>AD16</td>
<td>+3.3V</td>
<td>C/BE2*</td>
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<td>15</td>
<td>AD18</td>
<td>+3.3V</td>
<td>AD17</td>
<td>GND</td>
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<td>AD21</td>
<td>AD20</td>
<td>GND</td>
<td>AD19</td>
</tr>
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<td>+3.3V</td>
<td>AD23</td>
<td>AD22</td>
<td>+3.3V</td>
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<td>IDSEL2</td>
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<td>AD24</td>
<td>C/BE3*</td>
<td>VI/O</td>
<td>IDSEL3</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>AD26</td>
<td>AD25</td>
<td>GND</td>
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<td>21</td>
<td>AD29</td>
<td>+5V</td>
<td>AD28</td>
<td>AD27</td>
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<td>+5V</td>
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<td>GND</td>
<td>AD31</td>
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<td>REQ0*</td>
<td>GND</td>
<td>REQ1*</td>
<td>VI/O</td>
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**Notes:**
1. The shaded area denotes power or ground signals.
2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding.
### Table 4: PC/104 Bus (Reference Only)

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PC/104-Plus Specification Version 1.2 — Page B-3