AN754

Understanding Microchip's CAN Module Bit Timing

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INTRODUCTION

The Controller Area Network (CAN) protocol is an asynchronous serial bus with Non-Return to Zero (NRZ) bit coding designed for fast, robust communications in harsh environments, such as automotive and industrial applications. The CAN protocol allows the user to program the bit rate, the sample point of the bit, and the number of times the bit is sampled. With these features, the network can be optimized for a given application.

There are relationships between bit timing parameters, the physical bus propagation delays, and the oscillator tolerances throughout the system. This application note investigates these relationships as they pertain to Microchip's CAN module and assists in optimizing the bit timing for given physical system attributes.

THE CAN BIT TIME

The CAN bit time is made up of non-overlapping segments. Each of these segments are made up of integer units called Time Quanta (TQ) and are explained later in this application note. The Nominal Bit Rate (NBR) is defined in the CAN specification as the number of bits per second transmitted by an ideal transmitter with no resynchronization and can be described with the equation:

$$NBR = f_{bit} = \frac{1}{t_{bit}}$$

Nominal Bit Time

The Nominal Bit Time (NBT), or t_{bit}, is made up of non-overlapping segments (Figure 1), therefore, the NBT is the summation of the following segments:

$$t_{bit} = t_{SyncSeg} + t_{PropSeg} + t_{PS1} + t_{PS2}$$

Associated with the NBT are the Sample Point, Synchronization Jump Width (SJW), and Information Processing Time (IPT), which are explained later.

SYNCHRONIZATION SEGMENT

The Synchronization Segment (SyncSeg) is the first segment in the NBT and is used to synchronize the nodes on the bus. Bit edges are expected to occur within the SyncSeg. This segment is fixed at 1TQ.

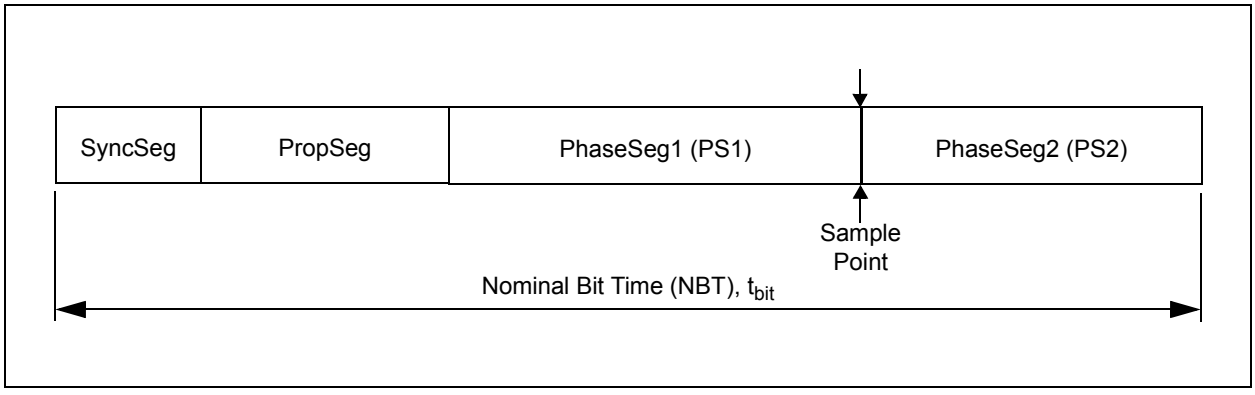
PROPAGATION SEGMENT

The Propagation Segment (PropSeg) exists to compensate for physical delays between nodes. The propagation delay is defined as twice the sum of the signal's propagation time on the bus line, including the delays associated with the bus driver. The PropSeg is programmable from 1 - 8TQ.

PHASE SEGMENT 1 AND PHASE SEGMENT 2

The two phase segments, PS1 and PS2 are used to compensate for edge phase errors on the bus. PS1 can be lengthened or PS2 can be shortened by resyncronization. PS1 is programmable from 1 - 8TQ and PS2 is programmable from 2 - 8TQ.

FIGURE 1: CAN BIT TIME SEGMENTS



SAMPLE POINT

The sample point is the point in the bit time in which the logic level is read and interpreted. The sample point is located at the end of phase segment 1. The exception to this rule is, if the sample mode is configured to sample three times per bit. In this case, the bit is still sampled at the end of PS1, however, two additional samples are taken at one-half TQ intervals prior to the end of PS1 and the value of the bit is determined by a majority decision.

INFORMATION PROCESSING TIME

The Information Processing Time (IPT) is the time required for the logic to determine the bit level of a sampled bit. The IPT begins at the sample point, is measured in TQ and is fixed at 2TQ for the Microchip CAN module. Since phase segment 2 also begins at the sample point and is the last segment in the bit time, it is required that PS2 minimum is not less than the IPT.

Therefore:

$$PS2_{min} = IPT = 2TQ$$

SYNCHRONIZATION JUMP WIDTH

The Synchronization Jump Width (SJW) adjusts the bit clock as necessary by 1 - 4TQ (as configured) to maintain synchronization with the transmitted message. More on synchronization is covered later.

Time Quantum

Each of the segments that make up a bit time are made up of integer units called Time Quanta (TQ). The length of each Time Quantum is based on the oscillator period (t_{OSC}). The base TQ equals twice the oscillator period. Figure 2 shows how the bit period is derived from T_{OSC} and TQ. The TQ length equals one TQ Clock period (t_{BRPCLK}), which is programmable using a programmable prescaler named the Baud Rate Prescaler (BRP). This is shown in the following equation:

$$TQ = 2 \cdot BRP \cdot T_{OSC} = \frac{2 \cdot BRP}{F_{OSC}}$$

Where: BRP equals the configuration as shown in Figure 3.

Bit Timing Control Registers

The CAN Bit Timing Control (CNF) registers are the three registers that configure the CAN bit time. Figure 3 details the function of the CNF registers.

By adjusting the length of the TQ (t_{TQ}) and the number of TQs in each segment, both the nominal bit time and the sample point can easily be configured as desired.

PROGRAMMING THE TIMING SEGMENTS

The are several requirements for programming the CAN bit timing segments.

1. PropSeg + PS1 ≥ PS2
2. PropSeg + PS1 ≥ t_{PROP}
3. PS2 > SJW

FIGURE 2: TQ AND THE BIT PERIOD

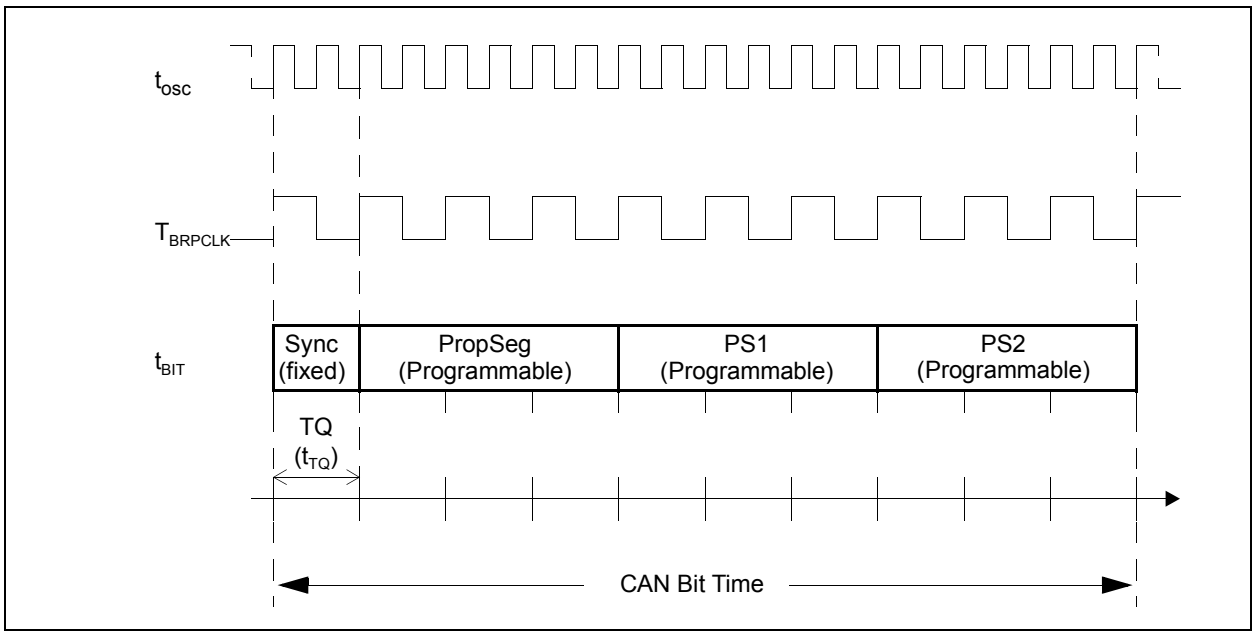


FIGURE 3: CAN BIT TIMING CONTROL REGISTERS (MCP2510 CNF REGISTERS)

CNF1

SJW.1	SJW.0	BRP.5	BRP.4	BRP.3	BRP.2	BRP.1	BRP.0

bit 7 bit 0

SJW<1:0> (Synchronization Jump Width Length as measured in TQ):
11 = 4TQ
10 = 3TQ
01 = 2TQ
00 = 1TQ

BRP<5:0> (Baud Rate Prescaler TQ length as a multiple of t_{osc})
111111 = TQ = 2 x 64 x t_{OSC}
. .
. .
. .
000010 = TQ = 2 x 3 x t_{OSC}
000001 = TQ = 2 x 2 x t_{OSC}
000000 = TQ = 2 x 1 x t_{OSC}

CNF2

BTLMODE	SAM	PS1.2	PS1.1	PS1.0	PRSEG.2	PRSEG.1	PRSEG.0

bit 7 bit 0

BTLMODE (Determines how PS2 is calculated)
1 = PS2 is determined by CNF3.PS2<2:0>
0 = PS2 is the greater of PS1 and the Information Processing Time (IPT)

SAM (Configures the sample point as one sample or three samples
1 = Sample three times per bit
0 = Sample once per bit

PS1<2:0> (Configures Phase Segment 1)
111 = 8TQ
. .
. .
001 = 2TQ
000 = 1TQ

PRSEG<2:0> (Configures the Propagation Segment)
111 = 8TQ
. .
. .
001 = 2TQ
000 = 1TQ

CNF3

---	WAKFIL	---	---	---	PHSEG22	PHSEG21	PHSEG20

bit 7 bit 0

WAKFIL (Enables/Disables the wakeup filter)
1 = Filter enabled
0 = Filter disabled

PS2<2:0> (Configures Phase Segment 2)
111 = 8TQ
. .
. .
001 = 2TQ
000 = Not Valid ($PS2_{MIN}$ = IPT = 2TQ)

SYNCHRONIZING THE BIT TIME

All nodes on the CAN bus must have the same nominal bit rate. Noise, phase shifts, and oscillator drift create situations where the nominal bit rate does not equal the actual bit rate in a real system. Therefore, the nodes must have a method for achieving and maintaining synchronization with bus messages.

Oscillator Tolerance

The bit timing for each node in a CAN system is derived from the reference frequency (f_{OSC}) of its node. This creates a situation where phase shifting and oscillator drift will occur between nodes due to less than ideal oscillator tolerances between the nodes.

The CAN specification indicates that the worst case oscillator tolerance is 1.58% and is only suitable for low bit rates (125 kb/s or less). This application note does not cover oscillator tolerances in detail, however, the references at the end of this application note provide more information on the subject.

Propagation Delay

The CAN protocol has defined a recessive (logic 1) and dominant (logic 0) state to implement a non-destructive bit-wise arbitration scheme. It is this arbitration methodology that is affected the most by propagation delays. Each node involved with arbitration must be able to sample each bit level within the same bit time. For example, if two nodes at opposite ends of the bus start to transmit their messages at the same time, they must arbitrate for control of the bus. This arbitration is only effective if both nodes are able to sample during the same bit time. Figure 4 shows a one-way propagation delay between two nodes. Extreme propagation delays (beyond the sample point) will result in invalid arbitration. This implies that bus lengths are limited at given CAN data rates.

A CAN system's propagation delay is calculated as being a signal's round trip time on the physical bus (t_{bus}), the output driver delay (t_{drv}), and the input comparator delay (t_{cmp}). Assuming all nodes in the system have similar component delays, the propagation delay is explained mathematically as:

$$t_{prop} = 2 \cdot (t_{bus} + t_{cmp} + t_{drv})$$

Synchronization

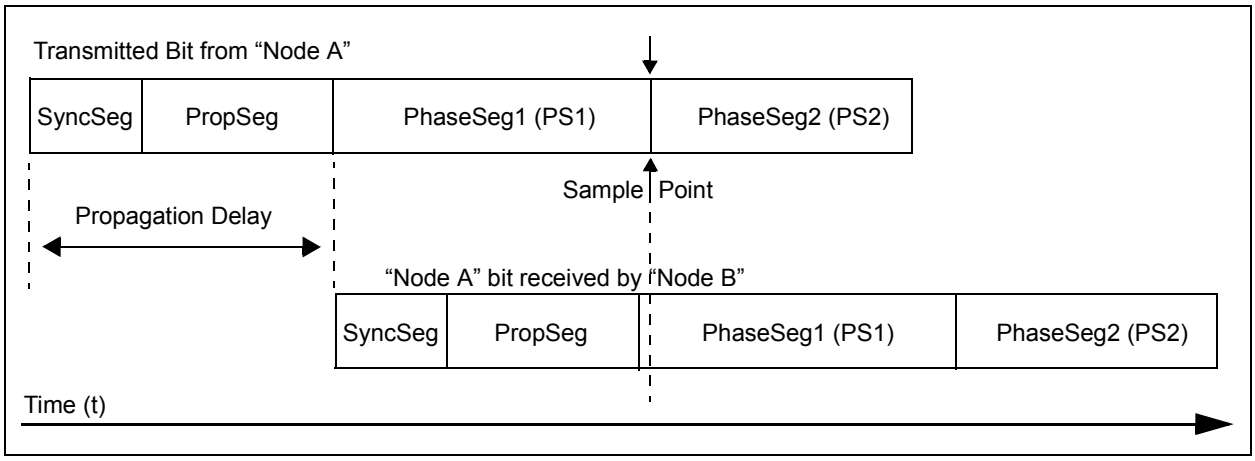
All nodes on a given CAN bus must have the same NBT. The NRZ bit coding does not encode a clock into the message. The receivers must synchronize to the transmitted data stream to insure messages are properly decoded. There are two methods used for achieving and maintaining synchronization.

HARD SYNCHRONIZATION

Hard Synchronization only occurs on the first recessive-to-dominant (logic "1" to "0") edge during a bus idle condition, which indicates a Start-of-Frame (SOF) condition. Hard synchronization causes the bit timing counter to be reset to the SyncSeg which causes the edge to lie within the SyncSeg. At this point, all of the receivers will be synchronized to the transmitter.

Hard synchronization occurs only once during a message. Also, resynchronization may not occur during the same bit time (SOF) that hard synchronization occurred.

FIGURE 4: ONE WAY PROPAGATION DELAY



RESYNCHRONIZATION

Resynchronization is implemented to maintain the initial synchronization that was established by the hard synchronization. Without resynchronization, the receiving nodes could get out of synchronization due to oscillator drift between nodes.

Resynchronization is achieved by implementing a Digital Phase Lock Loop (DPLL) function which compares the ***actual*** position of a recessive-to-dominant edge on the bus to the position of the ***expected*** edge (within the SyncSeg) and adjusting the bit time as necessary.

The phase error of a bit is given by the position of the edge in relation to the SyncSeg, measured in TQ, and is defined as follows:

- e = 0; the edge lies within the SyncSeg.
- e > 0; the edge lies before the sample point. (TQ added to PS1).
- e < 0; the edge lies after the sample point of the previous bit. (TQ subtracted from PS2)

FIGURE 5: SYNCHRONIZING THE BIT TIME

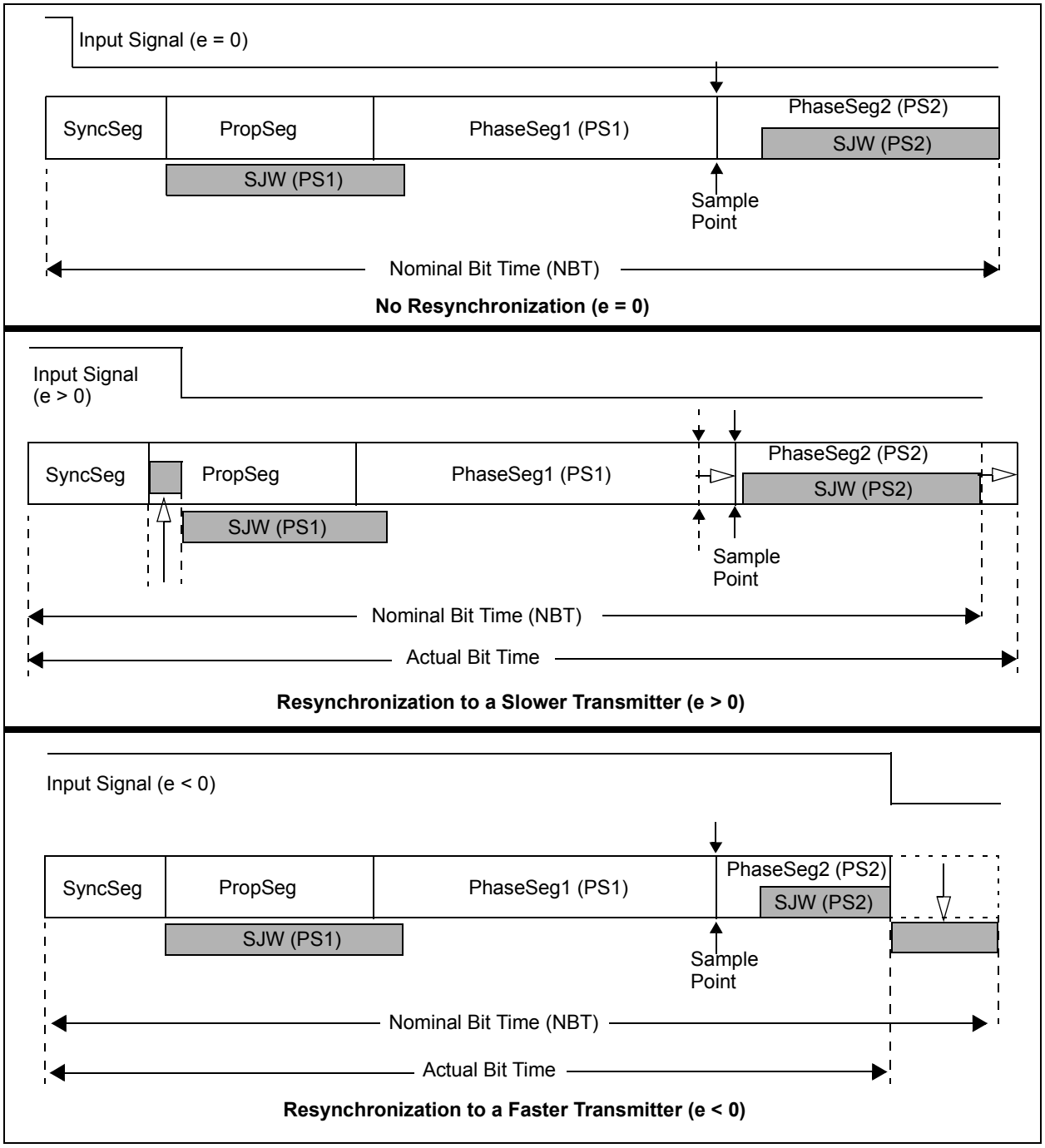


Figure 5 shows how phase errors, other than zero, cause the bit time to be lengthened or shortened.

Synchronization Rules:

1. Only recessive-to-dominant edges will be used for synchronization.
2. Only one synchronization within one bit time is allowed.
3. An edge will be used for synchronization only if the value at the previous sample point differs from the bus value immediately after the edge.
4. A transmitting node will not resynchronize on a positive phase error (e > 0). This implies that a transmitter will not resynchronize due to propagation delays of it's own transmitted message. The receivers will synchronize normally.
5. If the absolute magnitude of the phase error is greater than the SJW, then the appropriate phase segment will be adjusted by an amount equal to the SJW.

PUTTING IT ALL TOGETHER

As indicated previously, the CAN protocol implements a non-destructive bitwise arbitration scheme that allows multiple nodes to arbitrate for control of the bus. Therefore, it is necessary for all the nodes to detect/sample the bits within the same bit time. The relationship between propagation delay and oscillator tolerance effect both the CAN data rate and the bus length. Table 1 shows some commonly accepted bus lengths versus data rates.

This application note does not cover all of the details for configuring the bit time for all scenarios, however, some general methodologies for configuring the CAN bit time are covered.

TABLE 1: CAN BIT RATE VS. BUS LENGTH

Bit Rate (kb/s)	Bus Length (m)
1000	30
500	100
250	250
125	500
62.5	1000

Calculating Oscillator Tolerance for SJW

The bit stuffing rule guarantees that no more than five like bits in a row will be transmitted during a message frame. The only exception is at the end of the message that includes ten recessive bits (one ACK delimiter, seven end-of-frame bits, and three interframe space bits).

Resynchronization can only occur on recessive-to-dominant edges. This implies that there can be a maximum of ten bits between resynchronization due to bit stuffing (Figure 6).

The oscillator tolerance between the slowest node and the fastest node can be used to determine the minimum SJW. Assuming Node A is the slow node (longest bit time) and Node B is the fast node (shortest bit time):

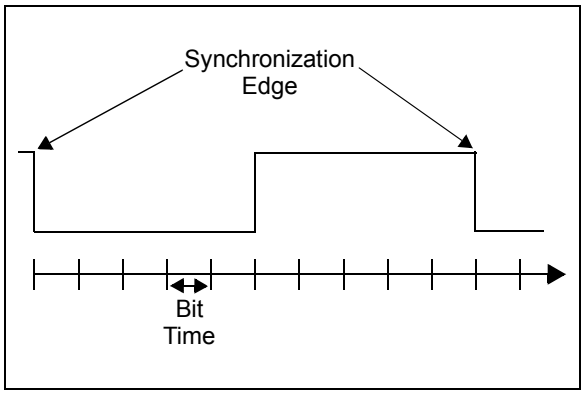
$$10t_{bit(A)} > 10t_{bit(B)} + t_{SJW(B)}$$

Where:

$t_{bit(n)}$ = bit time of node "n"

$t_{SJW(n)}$ = SJW of node "n"

FIGURE 6: MAXIMUM TIME BETWEEN SYNCHRONIZATION EDGES



EXAMPLE 1: Find Minimum SJW

Given:

Nominal Bit Time = 1 µs

Oscillator tolerance = 1.25%

Note: #TQ per bit = 8

Find SJW minimum:

$t_{bit(A)}$ = 1.01200 µs

$t_{bit(B)}$ = 0.98875 µs

$TQ_{(A)}$ = 126.563 ns

$TQ_{(B)}$ = 123.438 ns

Using equation above:

$t_{SJW(B)} > 10t_{bit(A)} - 10t_{bit(B)}$ = 0.250 µs

$\#TQ_{SJW} > t_{SJW(B)} / TQ_{(B)}$ = 250 ns / 123.44 ns = 2.025

$\#TQ_{SJW}$ = 3

Alternatively, the following equation can be used to maintain synchronization during normal bus operation:

$$SJW > (2\Delta f)(10NBT)$$

Solving for Oscillator Tolerance (Δf)

$$\Delta f < SJW / 20NBT$$

Configuring the Bit

In general, the longer the bus, the slower the maximum data rate due to propagation delays on the line. Increasing the oscillator tolerances between nodes can greatly amplify the relationship.

CAN system designers must take this relationship into consideration when defining the network. The following examples demonstrate bit timings for achieving maximum oscillator tolerance or maximum bit rate.

EXAMPLE 2: Maximum Oscillator Tolerance

The maximum oscillator tolerance for a maximum data rate is achieved when the phase segments 1 and 2 are equal to the maximum synchronization jump width (4TQ). Also, the propagation segment is minimum, indicating a short bus and fast transceiver.

As indicated earlier, the propagation delay is twice the delays of the bus, the receiver circuitry, and the driver.

$$t_{prop} = 2(t_{bus} + t_{cmp} + t_{drv})$$

Given:

t_{BUS} = 50 m @ 5.5 ns/m = 275 ns

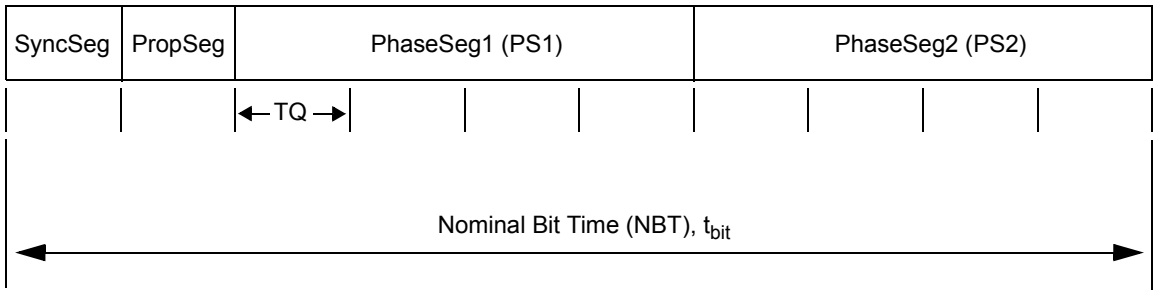
t_{CMP} = 40 ns

t_{DRV} = 60 ns

$t_{PROP} = 2(t_{BUS}+t_{CMP}+t_{DRV})$ = **750 ns**

Since the propagation segment is used to compensate for propagation delays and must be set to the minimum 1TQ, the implied time quantum = t_{PROP} = 750 ns. Figure 7 shows the bit timing.

FIGURE 7: BIT TIMING FOR MAXIMUM OSCILLATOR TOLERANCE



TQ = t_{PROP} = 750 ns
t_{bit} = 10TQ = 7.5 µs ⟶ 133.3 kb/s
SyncSeg = 1TQ
PropSeg = t_{PROP} = 1TQ
PS1 = SJW_{MAX} = 4TQ
PS2 = SJW_{MAX} = 4TQ
SJW_{MAX} = 0.4NBT = 4TQ

EXAMPLE 3: Maximum Bit Rate

The previous example showed that for a given bus length, the maximum data rate is inversely affected, due to oscillator tolerance (as oscillator tolerance goes up, the data rate goes down). To achieve the maximum bit rate for a given bus length, the emphasis is placed on configuring the bit time for the propagation delays (i.e., adjusting PropSeg to maximum). The oscillator tolerance must be minimized.

Given the same delays as the previous example:

t_{BUS} = 50 m @ 5.5 ns/m = 275 ns

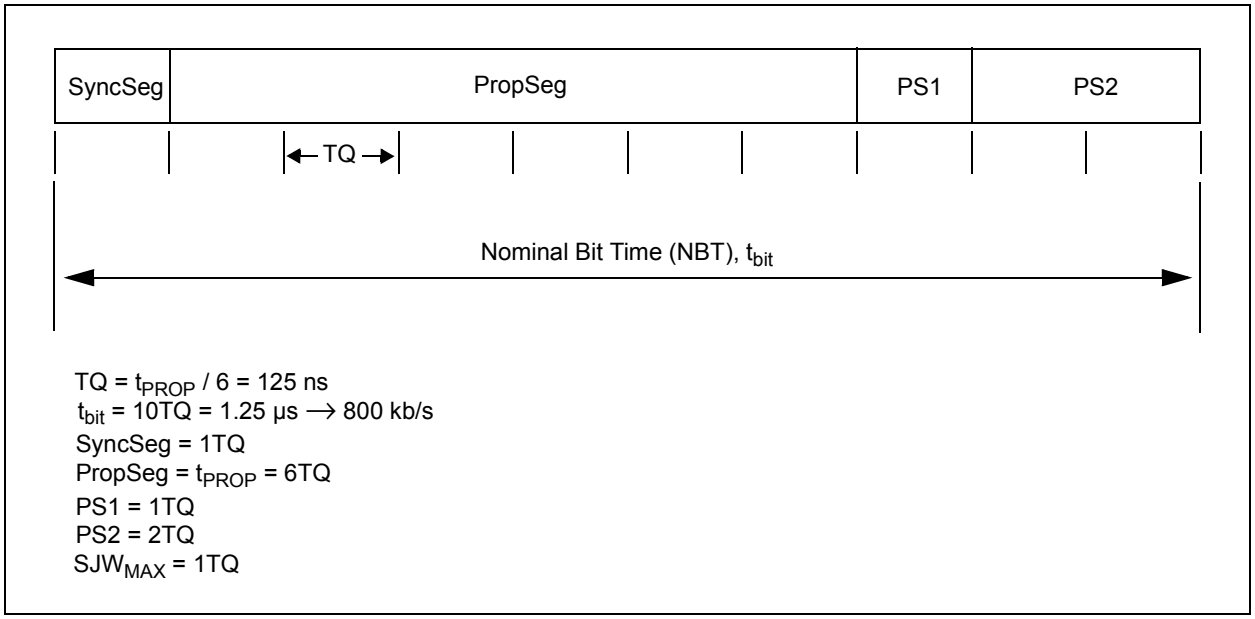
t_{CMP} = 40 ns

t_{DRV} = 60 ns

$t_{PROP} = 2(t_{BUS}+t_{CMP}+t_{DRV})$ = **750 ns**

Since the oscillator tolerance is minimum, the phase segments and SJW can be set to the minimum. Assuming the bit time is 10TQ total, the PropSeg can be set to 6TQ which sets TQ = 125 ns. Figure 8 shows the bit timing for maximum bit rate.

FIGURE 8: BIT TIMING FOR MAXIMUM BIT RATE



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CONCLUSION

Setting up CAN bit timing is not an arbitrary process. The system designer must be aware of the components that affect bit timing and compensate to get optimal performance across the network. For example, if the desired system uses oscillators with the maximum tolerance, the maximum bus length is reduced. Likewise, if maximum bus length is desired, the oscillator tolerances must be minimized. CAN data rates must also be considered because the data rate is a third variable that determines maximum length and maximum oscillator tolerances.

This application note should help assist system engineers design a controller area network for optimal performance based on requirements of the system.

DEFINITION OF TERMS

Dominant bit - Logic 0, overrides a recessive bit during arbitration.

Recessive bit - Logic 1.

CAN Node - A point in the network where CAN communications is connected.

Nominal Bit Time (NBT) - The length of a transmitted bit by an ideal transmitter with no resynchronization.

CAN - Controller Area Network.

Nominal Bit Rate (NBR) - The number of bits per second transmitted by an ideal transmitter.

Propagation Delay - Signals round trip time on the physical bus.

Hard Synchronization - Resets the receiving nodes bit timers. Occurs only at Start Of Frame (SOF).

Resynchronization - Maintains synchronization by adjusting the bits as needed.

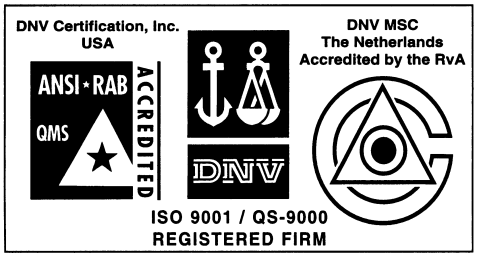
Information Processing Time (IPT) - The time required to determine the bit level. Begins at the sample point.

Start Of Frame (SOF) - The first dominate bit during bus idle. Indicates a start of frame.

Sample Point - Position within the bit where the logic level is sampled.

NOTES:

Trademarks



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