

Reference Manual

DOC. REV. 9/15/2011

Newt (VL-EPIC-17)

DMP Vortex-based SBC with
Ethernet, USB, Serial,
CompactFlash, eUSB, Analog +
Digital I/O, and SPX™



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Product Revision Notes

Revision 1.00 – Commercial release.

Support

The VL-EPIC-17 support page, at <http://www.versalogic.com/private/Newtsupport.asp>, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Datasheets and manufacturers' links for chips used in this product
- Photograph of the circuit board
- BIOS information and upgrades

This is a private page for VL-EPIC-17 users that can be accessed only by entering this address directly. It cannot be reached from the public VersaLogic website.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

[VersaTech KnowledgeBase](#)

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Description

FEATURES AND CONSTRUCTION

The Newt (VL-EPIC-17) is a feature-packed single board computer (SBC). It is designed for OEM control projects requiring high reliability and longevity (product lifespan). Its features include:

- DMP Vortex86DX System-on-Chip (SoC) x86 processor
- 256 MB (EA) or 512 MB (EB) soldered-on DDR2 RAM
- One (EA) or two (EB) 10BaseT/100BaseTX Ethernet
- PC/104-*Plus* expansion interface
- Three (EA) or four (EB) USB 1.1/2.0 Host channels
- Industrial I/O
 - 12-bit analog inputs and outputs
 - Eight (EA) or sixteen (EB) analog inputs
 - Four (EA) or eight (EB) analog outputs
 - Thirty-two digital I/O lines
- IDE controller (ATA/66, Ultra ATA/66, ATA-5, UDMA 3-4), one channel, up to two devices
- Four COM ports: two RS-232, two RS-232/422/485
- CompactFlash socket and eUSB interface (EA)
- Console redirection to COM port or video expansion with EPM-VID-3 or EPM-V4 via PC/104-*Plus* interface
- SPX interface supports up to four external SPI devices either of user design or any of the SPX series of expansion boards, with clock frequencies from 1–8 MHz
- TVS devices for ESD protection
- Two watchdog timers
- PS/2 keyboard and mouse interface
- Field upgradeable BIOS with OEM enhancements
- Battery-backed real-time clock
- V_{CC} sensing reset circuit
- RoHS compliant
- Extended temperature operation
- Customization available

The VL-EPIC-17 is compatible with popular operating systems including Windows XP/XPe/CE, Linux, VxWorks, and QNX (see the [VersaLogic OS Compatibility Chart](#)). Note: The Newt does not meet the minimum system requirements for Windows 7 or Windows Embedded Standard 7 (WES7).

The VL-EPIC-17 features high-reliability design and construction, including voltage sensing reset circuits and self-resetting fuses on the +5V supplies to the user I/O connectors.

VL-EPIC-17 boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional SBC.

VL-EPIC-17 FEATURE COMPARISON

The following table shows some key feature differences among standard and custom VL-EPIC-17 models.

Table 1: VL-EPIC-17 Model Comparison

<i>Model</i>	<i>RAM</i>	<i>Ethernet</i>		<i>USB Host</i>	<i>Industrial I/O</i>		<i>Flash</i>
		<i>Ports</i>	<i>Connector</i>		<i>A/D</i>	<i>D/A</i>	
VL-EPIC-17EA	256 MB	1	RJ45	3	8	4	CompactFlash eUSB
VL-EPIC-17EB	512 MB	2	RJ45	4	16	8	CompactFlash
VL-EPIC-17EC	256 MB	1	Ruggedized 8-pin latching	3	8	4	CompactFlash eUSB
VL-EPIC-17ED	512 MB	2	Ruggedized 8-pin latching	4	16	8	CompactFlash

Technical Specifications

Specifications are typical at 25°C with +5V supply unless otherwise noted.

Board Size:

4.5" x 6.5" (EPIC standard)

Storage Temperature:

-40° to +85°C

Operating Temperature:

-40° to +85°C, no airflow

Power Requirements: +5V with 256 MB RAM (EA/EC) or 512 MB RAM (EB/ED), Ethernet, keyboard, mouse running Windows XP, no video card

VL-EPIC-17EA/EC: 0.52A @ 5V (2.60W) idle

VL-EPIC-17EB/ED: 0.62A @ 5V (3.10W) idle

+3.3V or ±12V may be required by some expansion modules

System Reset:

V_{CC} sensing, resets below 4.70V typ.

Watchdog timeout (warm/cold reset)

DRAM:

Soldered-on 256 MB (EA/EC) or 512 MB (EB/ED) FBGA-60 DDR2, 300 MHz

Video Interface:

None. Optional EPM-VID-3 or VL-EPM-V4 expansion Console redirection to COM port

IDE Interface:

One channel, 44-pin, 2 mm connector; supports up to and including ATA/66 interface; supports two parallel ATA IDE devices (hard drive, CD-ROM, CF, etc.)

Flash Storage:

CompactFlash socket, shares IDE channel, master or slave, supports DMA; eUSB interface (EA/EC)

Ethernet Interface:

Single (EA/EC) or dual (EB/ED) Ethernet; Autodetect 10BaseT / 100BaseT Ethernet controller built in to Vortex86DX, 12K transmit/receive buffer

COM 1/2 Interface:

RS-232, 16C550 compatible, 115 Kbps max.

COM 3/4 Interface:

RS-232/422/485, 16C550 compatible, 115 Kbps max., 4-wire RS-232 (only CTS and RTS handshaking)

USB:

Three (EA/EC) or four (EB/ED) USB 1.1/2.0 Host ports; eUSB interface (EA/EC)

Analog Input:

8 or 16-channel, 12-bit, single-ended
0 to +4.095V (1 mV per bit)
100 Ksps

Analog Output:

4 or 8-channel, 12-bit, single-ended
0V to 4.096V
100 Ksps

SPX:

Supports four external SPI chips of user design or any SPX series expansion board

Audio:

Speaker output

BIOS:

American Megatrends (AMI) BIOS with OEM enhancements.

Bus Speed:

PCI: 33.33 MHz

ISA: 8.33 MHz

Bus Compatibility:

PC/104-Plus - Full compliance

Weight:

VL-EPIC-17EA - 0.321 lbs (0.145 kg)

VL-EPIC-17EB - 0.347 lbs (0.157 kg)

Specifications are subject to change without notification.

Block Diagram

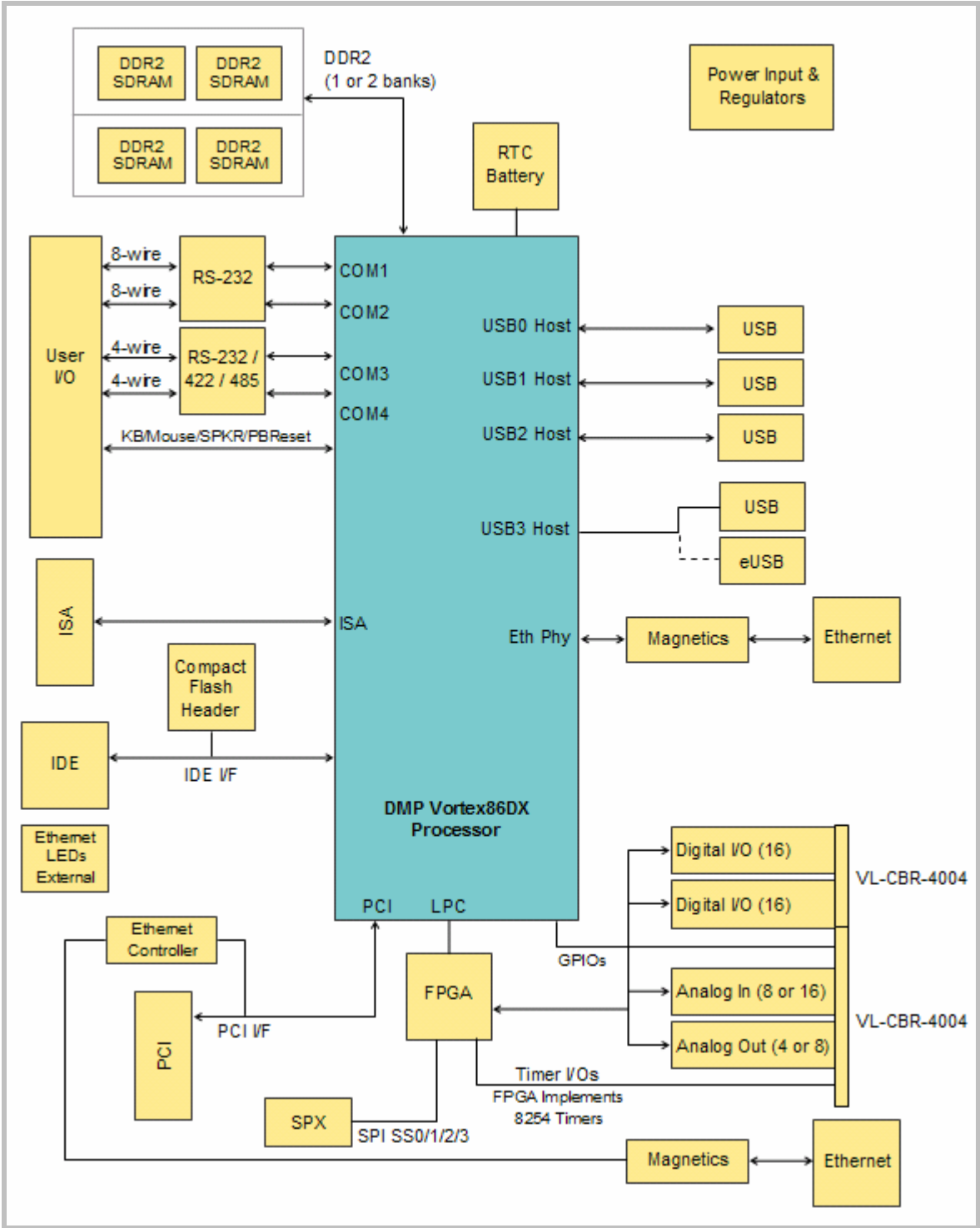


Figure 1. System Block Diagram

RoHS Compliance

The VL-EPIC-17 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corp. is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives, and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic antistatic envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the VL-EPIC-17.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

Technical Support

If you are unable to solve a problem after reading this manual, please visit the VL-EPIC-17 product support web page below. The support page provides links to component datasheets, device drivers, and BIOS and PLD code updates.

[VL-EPIC-17 Support Page](http://www.versalogic.com/private/newtsupport.asp)

<http://www.versalogic.com/private/newtsupport.asp>

The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-EPIC-17.

[VersaTech KnowledgeBase](#)

If you have further questions, contact VersaLogic Technical Support at (541) 485-8575. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

- Warranty Repair** All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.
- Non-warranty Repair** All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.
- Note:** Please mark the RMA number clearly on the outside of the box before returning.

Initial Configuration

The following components are recommended for a typical development system with the VL-EPIC-17 computer:

- ATX power supply
- USB or PS/2 keyboard and mouse (if PS/2, you will need the main I/O breakout board VL-CBR-5009 with adapter cable)
- IDE hard drive
- USB or IDE CD-ROM drive
- EPM-VID-3 or VL-EPM-V4 for video support

The following VersaLogic cables are recommended:

- VL-CBR-2022 – Power adapter cable
- VL-CBR-4406 – IDE data cable
- VL-CBR-4405 – IDE adapter board, if you are using drives with 40-pin connectors
- LVDS or SVGA video adapter cable

You will also need an operating system (OS) installation CD-ROM.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The VL-EPIC-17 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the VL-EPIC-17 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the VL-EPIC-17 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 2 shows a typical start-up configuration.

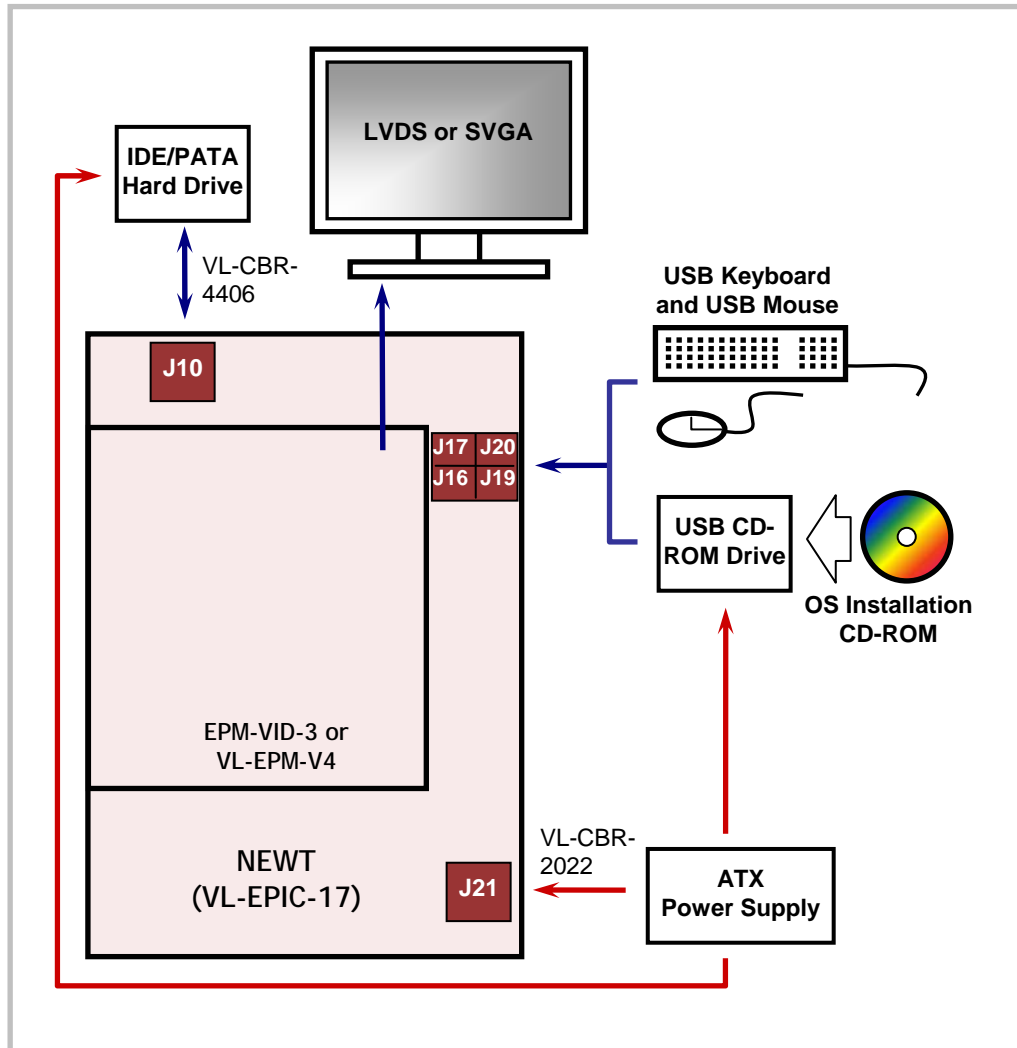


Figure 2. Typical Start-up Configuration

1. Attach Cables and Peripherals

- Install the video card on top of the VL-EPIC-17, configured for PCI Slot 0.
- Plug the LVDS or SVGA cable into the appropriate video card connector.
- Plug a USB keyboard and mouse into USB sockets J16, J17, J19, or J20. (A PS/2 keyboard and mouse can be plugged into the main I/O board VL-CBR-5009, which attaches to header J11.)
- Plug the hard drive data cable VL-CBR-4406 into socket J10. Attach a hard drive to a connector on the cable. If the hard drive is 3.5", use the 2 mm to 0.1" adapter VL-CBR-4405 to attach the IDE cable.
- Plug a USB CD-ROM drive into an available USB socket (J16, J17, J19, or J20). (If you are using an IDE CD-ROM drive, plug it into the VL-CBR-4406 data cable.)
- Attach an ATX power cable to any 3.5" drive (hard drive or CD-ROM drive).
- Set the hard drive jumper for master device operation and the CD-ROM drive jumper for slave device operation.

3. Attach Power

- Plug the power adapter cable VL-CBR-2022 into socket J21. Attach the motherboard connector of the ATX power supply to the adapter.

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EPIC-17 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present. (There might be a delay of several seconds before the video signal becomes present.)

6. Install Operating System

- Install the OS according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

Note: If you intend to operate the VL-EPIC-17 under Windows XP or Windows XP Embedded, be sure to use Service Pack 3 (SP3) for full support of the latest device features.

Operating System Installation

The standard PC architecture used on the VL-EPIC-17 makes the installation and use of most of the standard x86-based operating systems very simple. The operating systems listed on the [VersaLogic OS Compatibility Chart](#) use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular OS, or a link to the drivers, are available at the [VL-EPIC-17 Product Support web page](#).

CMOS Setup

The default CMOS Setup parameters for the VL-EPIC-17EA are shown below. Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown below. The factory default date will correspond to the BIOS build date. Settings will vary depending on the configuration of your VL-EPIC-17.

MAIN MENU

+-----+-----+	
System Overview	

AMIBIOS	
Version :08.00.15	
Build Date:11/26/10	
ID :1ADSV000	
Processor	
Vortex86DX A9121	
Speed :800MHz	
System Memory	
Size :256MB	
Speed :300MHz	
System Time [11:15:23]	
System Date [Wed 09/13/2011]	
	↔ Select Screen
	↑↓ Select Item
	+ - Change Field
	Tab Select Field
	F1 General Help
	F10 Save and Exit
	ESC Exit
+-----+-----+	

ADVANCED MENU

+-----+-----+	
Advanced Settings	

WARNING: Setting wrong values in below sections may cause system to malfunction.	
> Board Configuration	
> CPU Configuration	
> IDE Configuration	
> Remote Access Configuration	
> USB Configuration	
SB LAN [Enabled]	
SB MAC Address [00 1B EB 00 74 35]	
SB LAN Boot [Disabled]	
CPU Frequency Adjustment [Disabled]	
DDRII/PCI Frequency Adjustment [Disabled]	
	↔ Select Screen
	↑↓ Select Item
	Enter Go to Sub Screen
	F1 General Help
	F10 Save and Exit
	ESC Exit
+-----+-----+	

Advanced > Board Configuration

<pre> Chip Serial Number :C2 00 00 01 0A 01 </pre>		
<pre> D00716 PI-23257 I-110422006 1119 1045R100.ROM </pre>		<pre> ↔ Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit </pre>

Advanced > CPU Configuration

<pre> CPU Configuration ----- Module Version - 00.01 Manufacturer: DMP Brand String: Vortex86DX A9121 Frequency : 800MHz Cache L1 : 16 KB L1 Cache [Enabled] Cache L2 : 256 KB L2 Cache [Write-Thru] L2 Cache Fetch Line Size [4 DWORD] CPU Speed Setting By [Divide By 1] CPU Fast Decode Cycle [Normal] </pre>		<pre> Options Disabled Enabled </pre>
		<pre> ↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit </pre>

Advanced > IDE Configuration

IDE Configuration		Options
OnBoard PCI IDE Controller	[Both]	Disabled Primary Secondary Both
> Primary IDE Master	[Hard Disk]	
> Primary IDE Slave	[Hard Disk]	
Hard Disk Write Protect	[Disabled]	
IDE Detect Time Out (Sec)	[5]	
ATA (PI) 80Pin Cable Detection	[Host & Device]	
IDE Operate Mode	[Legacy Mode]	↔ Select Screen
PCI IDE BusMaster	[Enabled]	↑↓ Select Item
Hard Disk Delay	[2 Second]	+ - Change Option
Standard IDE Compatible	[Disabled]	F1 General Help
		F10 Save and Exit
		ESC Exit

Advanced > IDE Configuration > IDE Master/Slave Configurations

Primary IDE Master		Options
Device	:Hard Disk	Not Installed
Vendor	:WDC WD800BB-56JKC0	Auto
Size	:80.0GB	CD/DVD
LBA Mode	:Supported	ARMD
Block Mode	:16Sectors	
PIO Mode	:4	
Async DMA	:MultiWord DMA-2	
Ultra DMA	:Ultra DMA-2	
S.M.A.R.T.	:Supported	
Type	[Auto]	↔ Select Screen
LBA/Large Mode	[Auto]	↑↓ Select Item
Block (Multi-Sector Transfer)	[Auto]	+ - Change Option
PIO Mode	[Auto]	F1 General Help
DMA Mode	[Auto]	F10 Save and Exit
S.M.A.R.T.	[Auto]	ESC Exit
32Bit Data Transfer	[Enabled]	

Advanced > Remote Access Configuration

----- Configure Remote Access type and parameters -----		Options
Remote Access	[Enabled]	Disabled Enabled
Serial port number	[COM1]	
Base Address, IRQ	[3F8h, 4]	
Serial Port Mode	[115200 8,n,1]	
Flow Control	[None]	
Redirection After BIOS POST	[Disabled]	
Terminal Type	[ANSI]	
VT-UTF8 Combo Key Support	[Enabled]	
Sredir Memory Display Delay	[No Delay]	
		↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

Advanced > USB Configuration

----- USB Configuration -----		Options
Module Version -	2.24.2-13.4	Disabled Enabled Auto
USB Devices Enabled :	3 Drives	
Legacy USB Support	[Enabled]	
USB 2.0 Controller Mode	[HiSpeed]	
BIOS EHCI Hand-Off	[Enabled]	
USB Beep Message	[Enabled]	
USB Port 0,1	[Enabled]	↔ Select Screen
USB Port 2,3	[Enabled]	↑↓ Select Item
USB Device	[Disabled]	Enter Go to Sub Screen
USB Hotplug Flash Drive	[Disabled]	F1 General Help
		F10 Save and Exit
> USB Mass Storage Device Configuration		ESC Exit

Advanced > USB Configuration > USB Mass Storage Device Configuration

USB Mass Storage Device Configuration		Options
USB Mass Storage Reset Delay	[20 Sec]	10 Sec 20 Sec 30 Sec 40 Sec
Device #1	Kingston DataTraveler	
Emulation Type	[Hard Disk]	
Device #2	Kingston DataTraveler	
Emulation Type	[Hard Disk]	
Device #3	SMART eUSB	
Emulation Type	[Hard Disk]	
		↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

PCIPNP MENU

Advanced PCI/PnP Settings		Options
WARNING: Setting wrong values in below sections may cause system to malfunction.		No Yes
Clear NVRAM	[No]	
Plug & Play O/S	[No]	
PCI Latency Timer	[128]	
Palette Snooping	[Disabled]	
IRQ3	[Reserved]	↔ Select Screen
IRQ4	[Reserved]	↑↓ Select Item
IRQ5	[Available]	+ - Change Option
IRQ6	[Available]	F1 General Help
IRQ7	[Available]	F10 Save and Exit
IRQ9	[Available]	ESC Exit
IRQ10	[Available]	
IRQ11	[Available]	
IRQ12	[Available]	
IRQ14	[Reserved]	
IRQ15	[Available]	
DMA Channel 0	[Available]	
DMA Channel 1	[Available]	
DMA Channel 3	[Available]	
DMA Channel 5	[Available]	
DMA Channel 6	[Available]	
DMA Channel 7	[Available]	
Reserved Memory Size	[Disabled]	
> IRQ Trigger Type Settings		

PCIPnP > IRQ Trigger Type Settings

IRQ Trigger Type Settings		Options
IRQ3	[Disabled]	Disabled
IRQ4	[Disabled]	Enabled
IRQ5	[Disabled]	
IRQ6	[Disabled]	
IRQ7	[Disabled]	
IRQ9	[Disabled]	
IRQ10	[Disabled]	
IRQ11	[Disabled]	
IRQ12	[Disabled]	
IRQ14	[Disabled]	
IRQ15	[Disabled]	
		↔ Select Screen
		↑↓ Select Item
		+ - Change Option
		F1 General Help
		F10 Save and Exit
		ESC Exit

BOOT MENU

Boot Settings	Configure Settings during System Boot.
> Boot Settings Configuration	
1st Boot Device [HDD:PM-WDC WD800BB-56JKC0]	
2nd Boot Device [HDD:PS-SILICONSYSTEMS INC 128MB]	
3rd Boot Device [USB:Kingston DataTraveler]	
4th Boot Device [USB:Kingston DataTraveler]	
5th Boot Device [USB:SMART eUSB]	
	↔ Select Screen
	↑↓ Select Item
	Enter Go to Sub Screen
	F1 General Help
	F10 Save and Exit
	ESC Exit

Boot > Boot Settings Configuration

Boot Settings Configuration		Options
Quick Boot	[Enabled]	Disabled
Quiet Boot	[Disabled]	Enabled
Bootup Num-Lock	[On]	
PS/2 Mouse Support	[Auto]	
Interrupt 19 Capture	[Enabled]	
Beep Function	[Disabled]	
Clear Base Memory	[Enabled]	
		↔ Select Screen
		↑↓ Select Item
		+ - Change Option
		F1 General Help
		F10 Save and Exit
		ESC Exit

SECURITY MENU

Security Settings		Options
Supervisor Password.....	Not Installed	
User Password.....	Not Installed	
Change Supervisor Password		
Change User Password		
Boot Sector Virus Protection	[Disabled]	
		↔ Select Screen
		↑↓ Select Item
		Enter Change
		F1 General Help
		F10 Save and Exit
		ESC Exit

CHIPSET MENU

<pre> Advanced Chipset Settings ----- WARNING: Setting wrong values in below sections may cause system to malfunction. > NorthBridge Configuration > SouthBridge Configuration </pre>	<pre> ↔ Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit </pre>
---	---

Chipset > NorthBridge Chipset Configuration

<pre> NorthBridge Chipset Configuration ----- DRAM Timing Setting By [BIOS] </pre>	<pre> Options Manual BIOS ↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit </pre>
---	---

Chipset > South Bridge Chipset Configuration

South Bridge Chipset Configuration	Options
P.O.S.T. Forward to SB COM1 [Disabled]	Disabled COM1
> ISA Configuration	
> Serial/Parallel Port Configuration	
> WatchDog Configuration	
	↔ Select Screen
	↑↓ Select Item
	+ - Change Option
	F1 General Help
	F10 Save and Exit
	ESC Exit

Chipset > South Bridge Chipset Configuration > ISA Configuration

ISA Configuration	Options
ISA Clock [8.3 MHz]	8.3MHz
DMA Operating Clock [4 MHz]	16.6MHz
ISA 16bits I/O wait-state [1 clock]	
ISA 8bits I/O wait-state [4 clock]	
ISA 16bits Memory wait-state [1 clock]	
ISA 8bits Memory wait-state [4 clock]	
	↔ Select Screen
	↑↓ Select Item
	+ - Change Option
	F1 General Help
	F10 Save and Exit
	ESC Exit

Chipset > South Bridge Chipset Configuration > Serial/Parallel Port Configuration

SB Serial Port1	[3F8]	Options
IRQ Select	[IRQ4]	Disabled
Baud Rate	[115200 BPS]	3F8
SB Serial Port2	[2F8]	2F8
IRQ Select	[IRQ3]	3E8
Baud Rate	[115200 BPS]	2E8
SB Serial Port3	[Disabled]	10
Serial Port Mode	[RS-232 4-wire]	
SB Serial Port4	[Disabled]	
Serial Port Mode	[RS-232 4-wire]	
		↔ Select Screen
		↑↓ Select Item
		+ - Change Option
		F1 General Help
		F10 Save and Exit
		ESC Exit

Chipset > South Bridge Chipset Configuration > WatchDog Configuration

WatchDog Configuration		Options
WatchDog0 Function	[Disabled]	Enabled
WatchDog1 Function	[Disabled]	Disabled
		↔ Select Screen
		↑↓ Select Item
		+ - Change Option
		F1 General Help
		F10 Save and Exit
		ESC Exit

EXIT MENU

<pre> Exit Options ----- Save Changes and Exit Discard Changes and Exit Discard Changes Load Optimal Defaults Load Failsafe Defaults Save Custom Defaults Load Custom Defaults </pre>	<pre> ↔ Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit </pre>
---	---

Dimensions and Mounting

VL-EPIC-17 DIMENSIONS

The VL-EPIC-17 complies with EPIC form factor standards. Dimensions are given below to help with pre-production planning and layout.

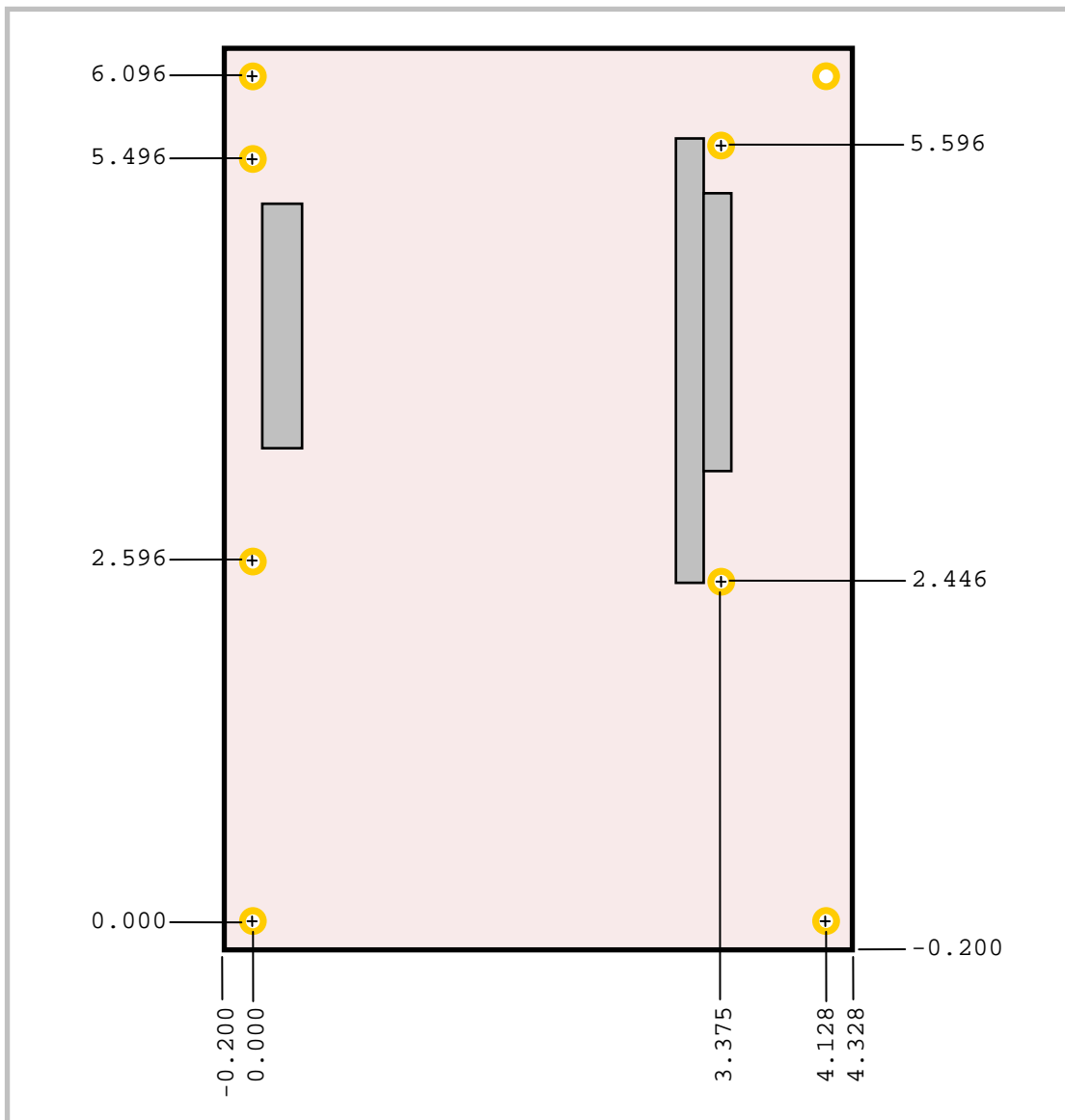


Figure 3. VL-EPIC-17 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

VL-CBR-5009 DIMENSIONS

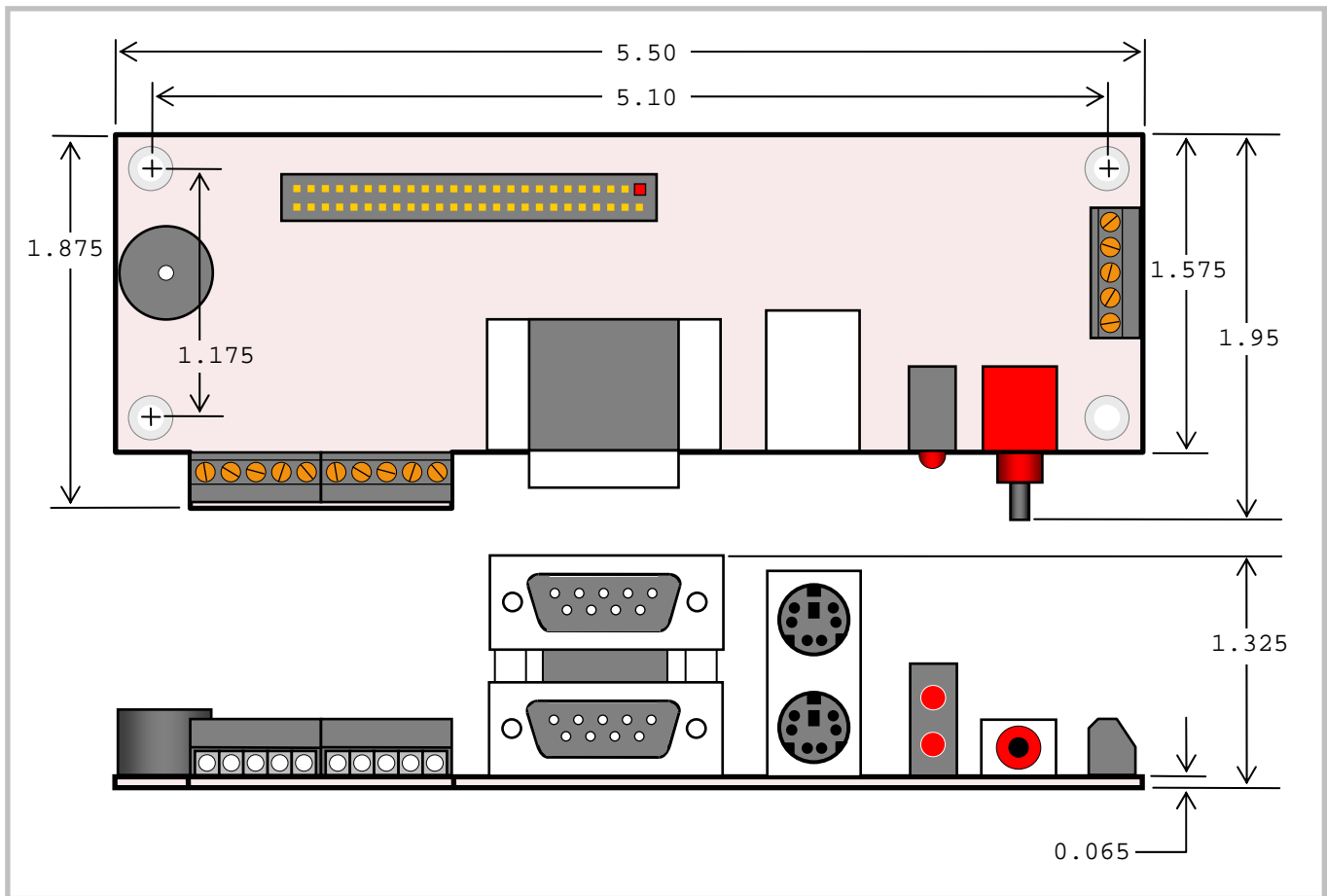


Figure 4. VL-CBR-5009 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

VL-CBR-4004 DIMENSIONS

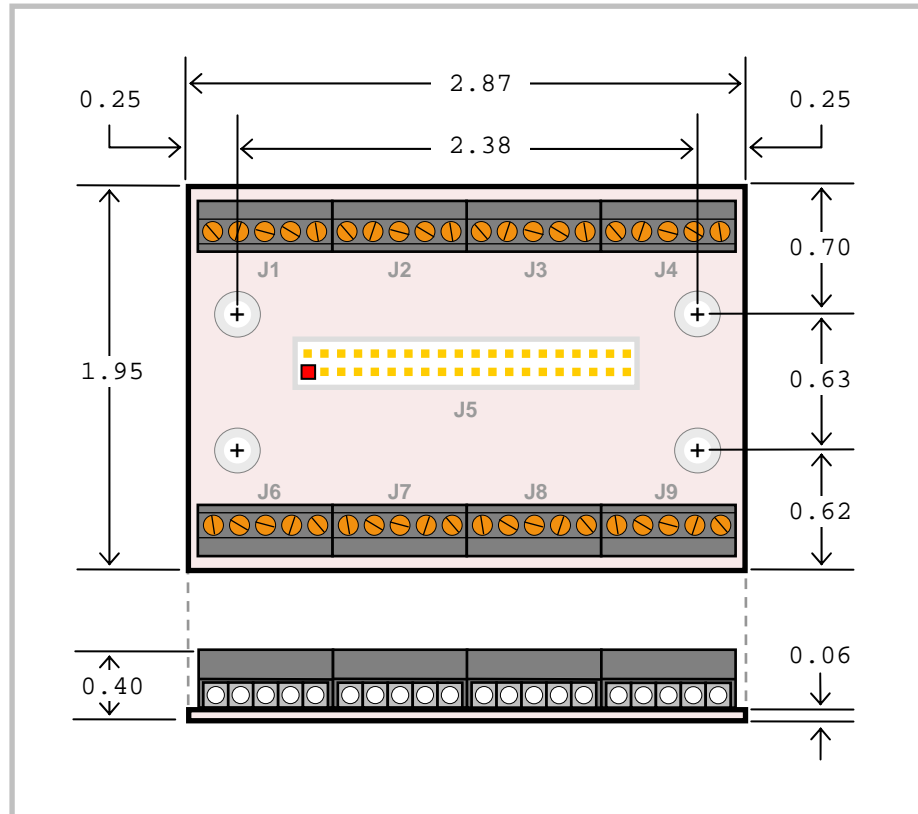


Figure 5. VL-CBR-4004 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The VL-EPIC-17 provides PC/104-Plus expansion with both PCI and ISA connectors so that expansion modules can be added to the top of the stack. PC/104 (ISA only) modules must not be positioned between the VL-EPIC-17 and any PC/104-Plus (PCI + ISA) or PCI-104 (PCI only) modules on the stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing. Four standoffs (B) must be used under the stack. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the PC/104 stack. Standoffs are secured to the top circuit board using pan head screws. Four standoffs and screws are available as part number VL-HDW-10x.

STANDOFF LOCATIONS

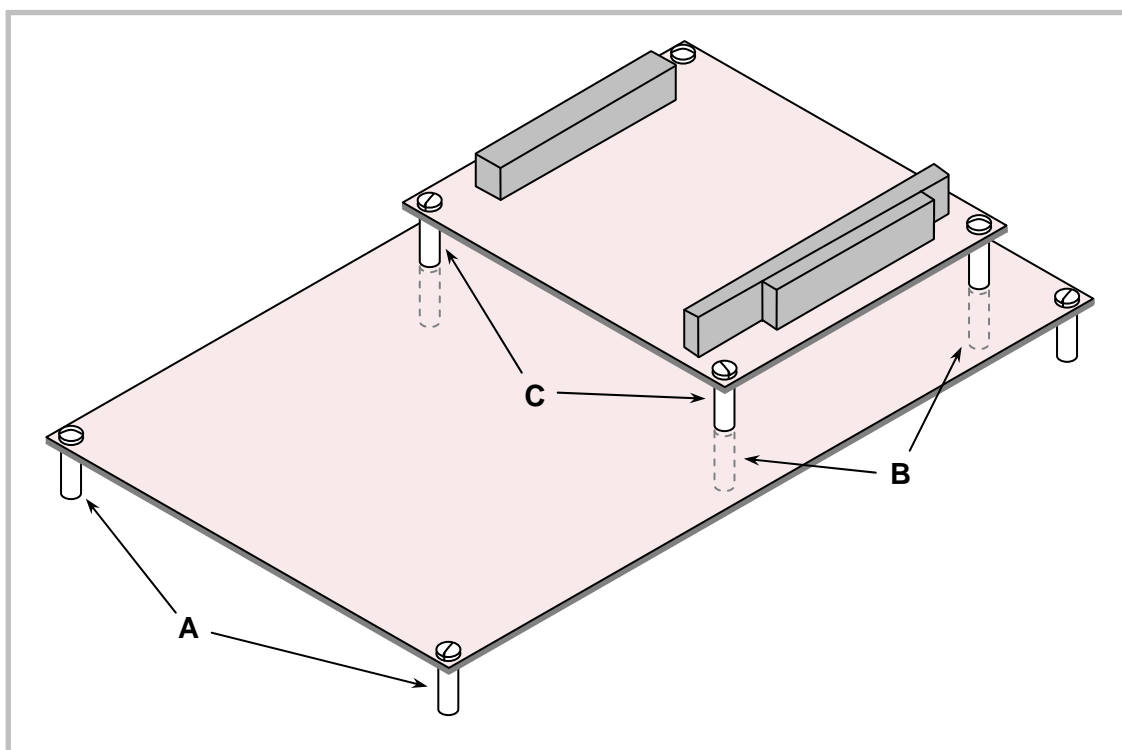


Figure 6. Stack Arrangement Example

External Connectors

VL-EPIC-17 CONNECTOR LOCATIONS – TOP

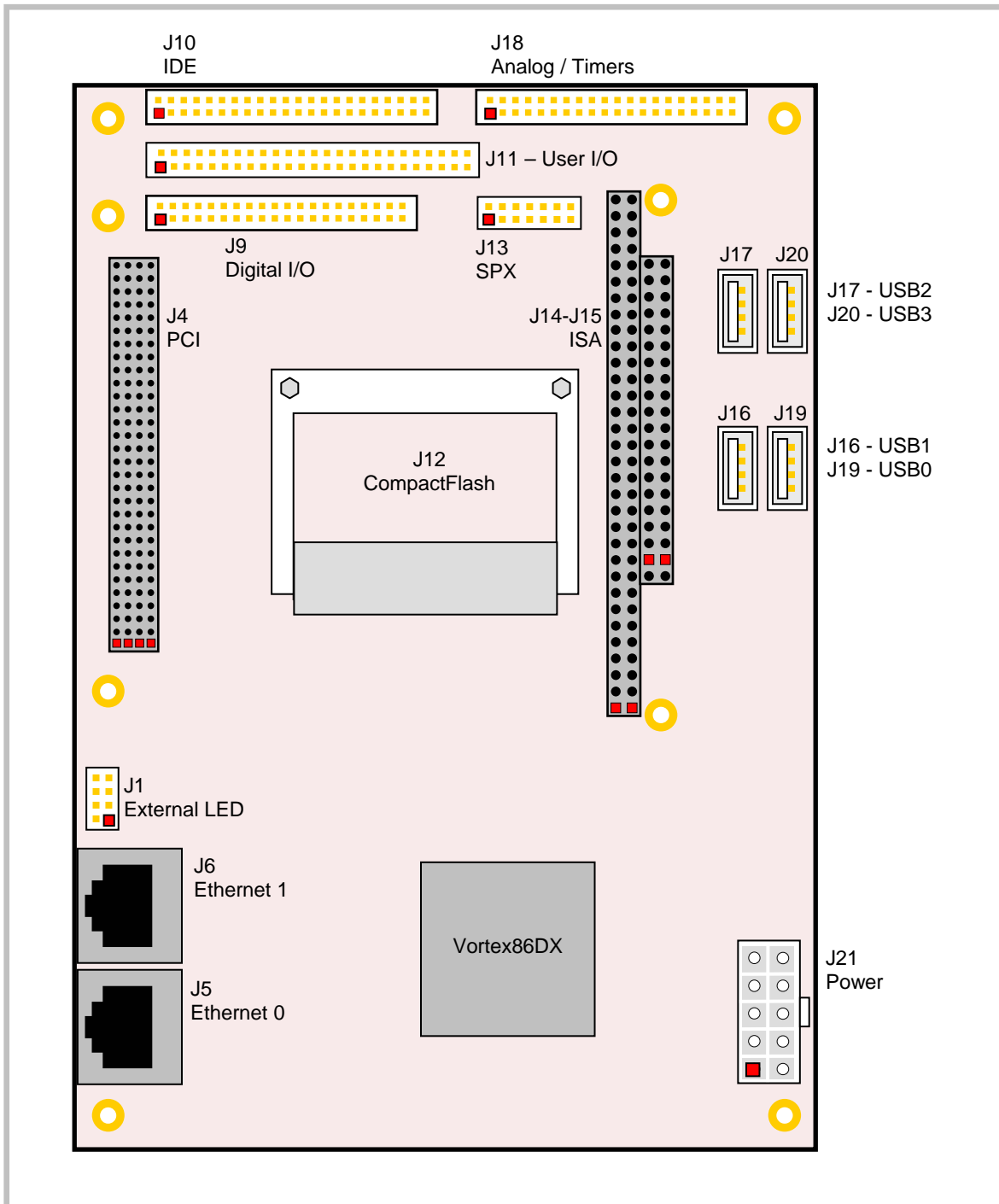


Figure 7. Connector Locations (Top)

VL-EPIC-17 CONNECTOR LOCATIONS – BOTTOM

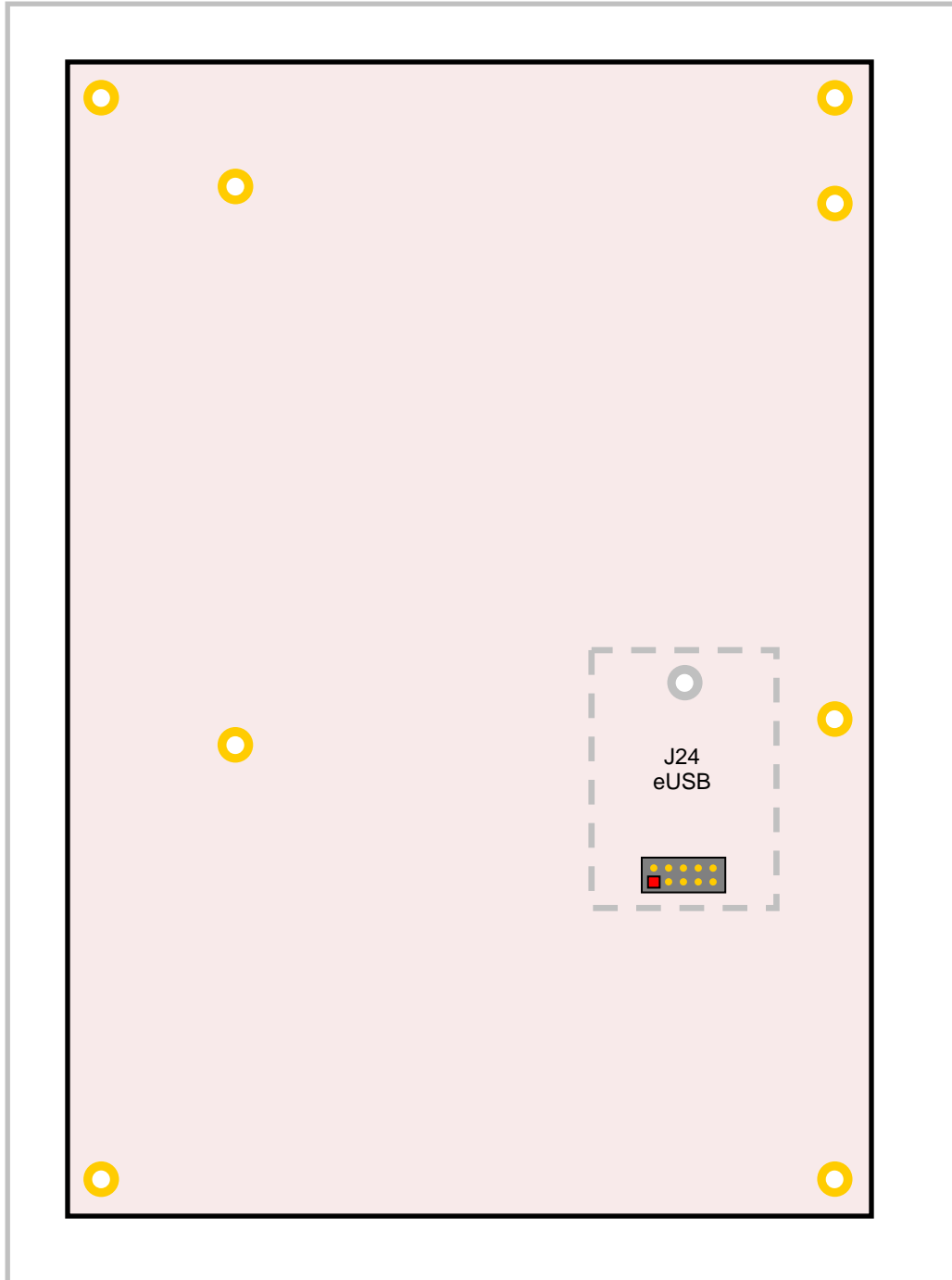


Figure 8. Connector Locations (Bottom)

VL-EPIC-17 CONNECTOR FUNCTIONS AND INTERFACE CABLES

Table 1 provides information about the function, mating connectors, and transition cables for VL-EPIC-17 connectors. Page numbers indicate where a detailed pinout or further information is available.

Table 2: Connector Functions and Interface Cables

Connector ¹	Function	Mating Connector	Transition Cable	Cable Description	Page	Pin 1 Location X Coord. Y Coord. ²	
J1	External Ethernet LEDs	—	—	—	40	46.7	104.2
J4	PCI	—	—	—	38	73.56	98.84
J5	Ethernet 0	RJ45	—	—	40	18.2772	98.3515
J6	Ethernet 1	RJ45	—	—	40	37.2968	98.3515
J9	Digital I/O	FCI 89361-340LF	VL-CBR-4004	12" 2 mm 40-pin to 40-pin IDC to VL-CBR-4004 board	49	138.9	97.0
J10	IDE interface	FCI 89947-144 (IDC)	VL-CBR-4406 VL-CBR-4405	12" 2mm IDE cable 2mm to 0.1" adapter	41	155.8	97.0
J11	COM ports, keyboard, mouse, GP timer inputs, power LED, pushbutton reset, PC speaker, LED	FCI 8947-350LF	VL-CBR-5009	12" 2mm latching 50-pin to 50-pin with breakout board	44	147.0	97.0
J12	CompactFlash Type I & II	—	—	—	42	116.53	71.535
J13	SPX	FCI 89361-714LF	VL-CBR-1401 or VL-CBR-1402	2mm 14-pin IDC, 2 or 4 SPX device cable	60	138.9	45.7
J14-J15	ISA	AMP 1375795-2	—	—	38	63.4 83.72 ³	24.21 19.13
J16	USB 1	Standard USB Type A	—	—	43	96.9	9.1
J17	USB 2	Standard USB Type A	—	—	43	121.4	9.1
J18	Analog/Timers I/O	FCI 89361-340LF	VL-CBR-4004	12" 2 mm 40-pin to 40-pin IDC to VL-CBR-4004 board	55	155.8	46.0
J19	USB 0	Standard USB Type A	—	—	43	96.9	1.1
J20	USB 3	Standard USB Type A	—	—	43	121.4	1.1
J21	Main power input	Molex 39-01-2100 Molex 39-00-0059 (10ea.)	VL-CBR-2022	6" ATX to EPIC power cable	34	7.348	4.611
J24	eUSB Flash Drive	—	—	—	43	42.9	78.4

1. Connectors J2, J3, J7, J8, J22, and J23 are not installed.

2. The PCB Origin is the mounting hole to the lower left as shown in Figure 3. All measurements in millimeters.

3. Pin A1.

CONNECTOR LOCATIONS – VL-CBR-5009

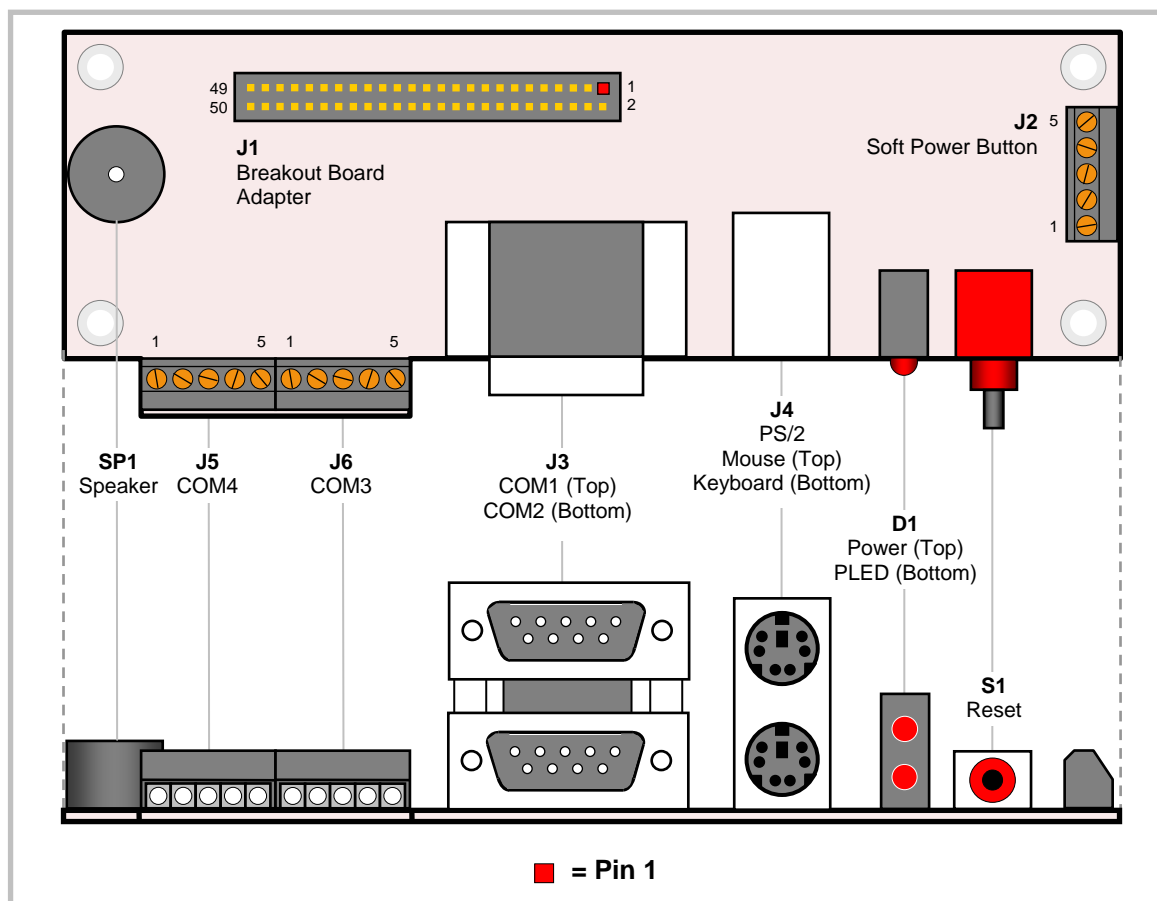


Figure 9. VL-CBR-5009 Connector Locations

VL-CBR-5009 CONNECTOR FUNCTIONS

Table 3: VL-CBR-5009 Connector Functions and Interface Cables

Connector / Component	Function	Part Number	Description
D1	Power and Programmable LEDs	Dialight 552-0211	LEDx2 T1 3/4 PC Mount Red/Red
J1	High Density Connector	FCI 98414-F06-50U	2 mm, 50-pin, keyed, latching header
J2	Soft Power Button Input	Conta-Clip 10250.4	5-pin screw terminal
J3	COM1, COM2	Kycon K42-E9P/P-A4N	Dual stacked DB-9 male
J4	PS/2 Keyboard and Mouse	Kycon KMDG-6S/6S-S4N	Dual stacked PS/2 female
J5	COM4	Conta-Clip 10250.4	5-pin screw terminal
J6	COM3	Conta-Clip 10250.4	5-pin screw terminal
S1	Reset Button	E-Switch 800SP9B7M6RE	Right angle momentary switch
SP1	Speaker	Challenge Electronics DBX05	Miniature PC speaker

VL-CBR-4004 CONNECTOR LOCATIONS

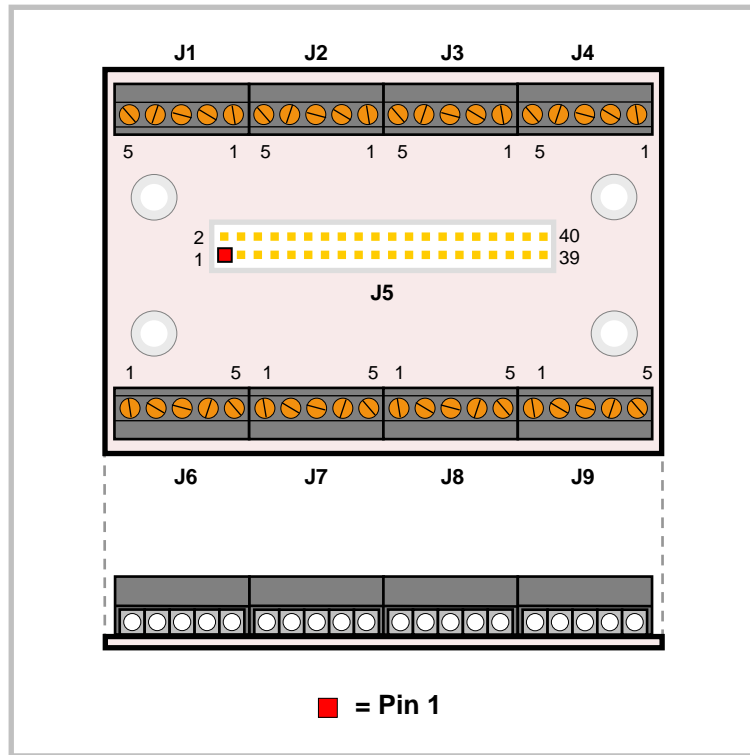


Figure 10. VL-CBR-4004 Connectors

Jumper Blocks

JUMPERS AS-SHIPED CONFIGURATION

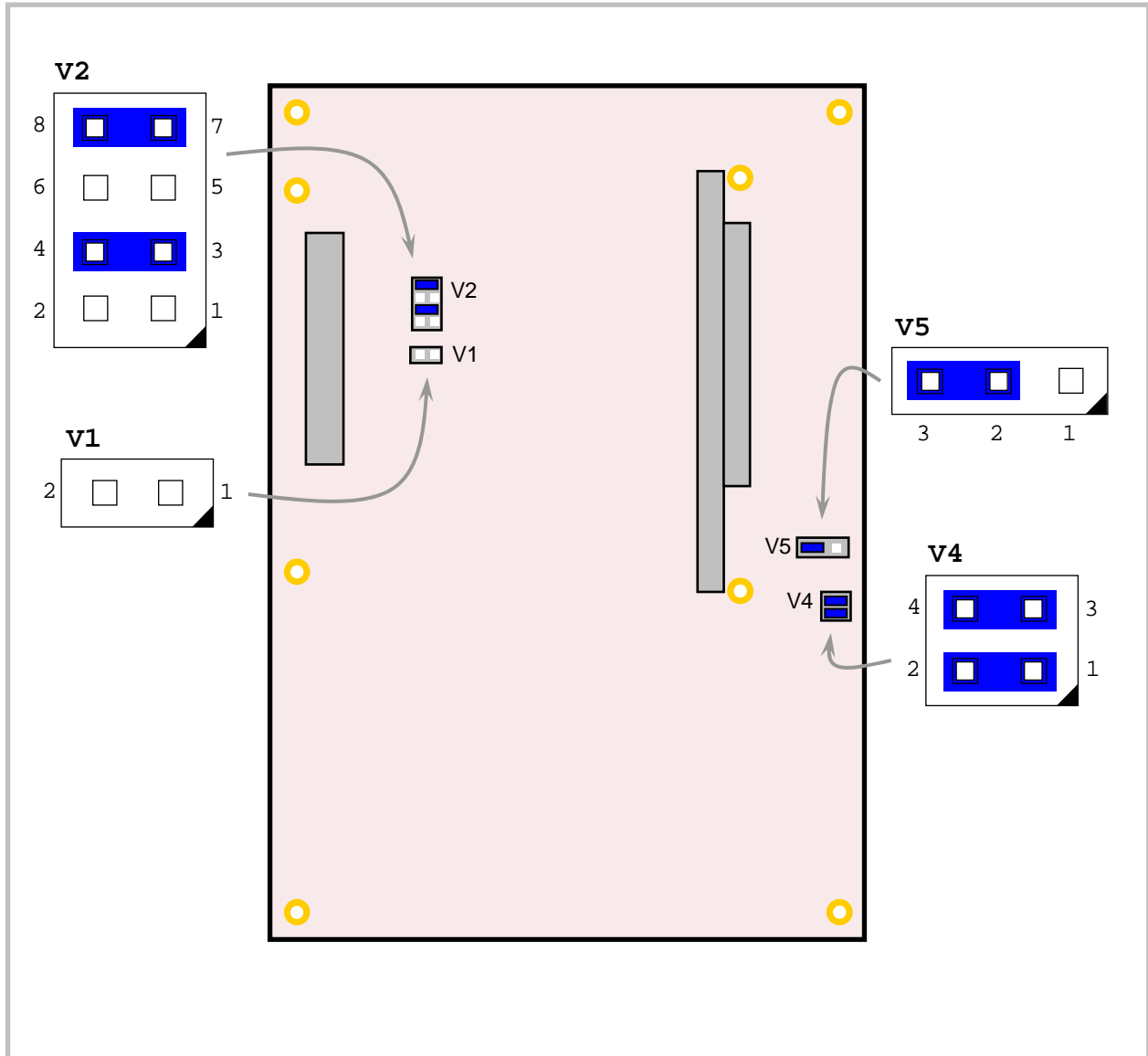


Figure 11. Jumper Block Locations

JUMPER SUMMARY

Table 4: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	CompactFlash Master/Slave Section In — Slave IDE Device Out — Master IDE Device	Out	42
V2[1-2] V2[3-4]	COM3 configuration [1-2] In and [3-4] In – RS-485 Endpoint [1-2] In and [3-4] Out – RS-232 [1-2] Out and [3-4] In – RS-422	[1-2] Out [3-4] In	45
V2[5-6] V2[7-8]	COM4 configuration [5-6] In and [7-8] In – RS-485 Endpoint [5-6] In and [7-8] Out – RS-232 [5-6] Out and [7-8] In – RS-422	[5-6] Out [7-8] In	45
V3	Jumper block not installed.	—	—
V4[1-2]	General Purpose Input Bit 1 In — Bit D7 in GPI register reads as 1 Out — Bit D7 in GPI register reads as 0	In	69
V4[3-4]	General Purpose Input Bit 2 In — Bit D0 in GPI register reads as 1 Out — Bit D0 in GPI register reads as 0	In	69
V5[1-2-3]	Battery Power Jumper [1-2] In – Discharge CMOS Memory [2-3] In – Standard Operation	[2-3] In	35

Power Supply

POWER CONNECTORS

Main power is applied to the VL-EPIC-17 through an EPIC-style 10-pin polarized connector at location J21.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5V_{DC} pins and all ground pins to prevent excess voltage drop.

Table 5: Main Power Connector Pinout

J21 Pin	Signal Name	Description
1	PS_ON	Soft Power Off
2	GND	Ground
3	GND	Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6	+5VSB	5V Standby
7	+5VDC	Power Input
8	+5VDC	Power Input
9	-12VDC	Power Input
10	GND	Ground

Note: The +3.3 V_{DC}, +12 V_{DC} and -12 V_{DC} inputs are necessary for expansion modules that require these voltages.

POWER REQUIREMENTS

The VL-EPIC-17 requires only +5V (±5%) for proper operation. The voltage required for the RS-232 ports is generated with an on-board DC/DC converter. Variable low-voltage supply circuits provide power to the CPU and other on-board devices.

The exact power requirements for the VL-EPICs-36 depend on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices, etc. For example, driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least +3V. If the voltage drops below +2V, contact the factory for a replacement (part number HB3/0-2SD). The life expectancy under normal use is approximately 10 years.

CPU

The Vortex86DX processor is an integrated System on Chip (SoC) containing an x86 processor. The CPU clock rate is 800 MHz. It integrates 3 2KB write through 4-way L1 cache, 4-way 256 KB L2 cache, PCI revision 2.1 with 32-bit bus interface at 33.33 MHz, DDR2, ROM controller, internal peripheral controllers (IPC) with DMA and interrupt timer/counter included, Fast Ethernet, UART (serial), USB 2.0 host, IDE controller, ISA bus, parallel port, and real-time clock.

System RAM

The VL-EPIC-17 has soldered on DDR2 SDRAM with the following characteristics:

- Storage Capacity VL-EPIC-17EA/EC – 256 MB
 VL-EPIC-17EB/ED – 512 MB
- Voltage +1.8V
- Speed 300 MHz DDR2

CMOS RAM

CLEARING CMOS RAM AND THE REAL-TIME CLOCK

You can move the V5 jumper to position [1-2] for a minimum of three seconds to erase the contents of CMOS RAM and the Real-Time Clock (RTC). When clearing the CMOS RAM:

1. Power off the VL-EPIC-17.
2. Move the jumper from V5[2-3] to V5[1-2] and leave it for four seconds.
3. Return the jumper to V5[2-3]. (The board will not boot if the jumper is not returned to this position.)
4. Power on the VL-EPIC-17.

Default BIOS Settings

The VL-EPIC-17 permits you to store user-defined BIOS settings. This allows you to retrieve those settings from cleared or corrupted CMOS RAM, or battery failure. All BIOS defaults can be changed, except the time and date. BIOS defaults can be updated with the BIOS Update Utility.

Warning! If BIOS default settings make the system unbootable and prevent the user from entering CMOS Setup, the VL-EPIC-17 needs to be serviced by the factory.

DEFAULT CMOS RAM SETUP VALUES

After CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

Real Time Clock

The VL-EPIC-17 features a battery-backed real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the Delete key during the early boot cycle, or F4 if operating in terminal mode) can be used to set the time and date of the real-time clock.

Watchdog Timer

The VL-EPIC-17 has two watchdog timers, which you can configure in CMOS Setup. The watchdog timers can be set to generate a reset, NMI, or an interrupt when timeout occurs. The expiration time can be set to a maximum of seconds. See the DMP Vortex86 Series Software Programming Reference on the [DMP Vortex86DX CPU Support Page](#) for instructions on programming the watchdog timer.

Console Redirection

The VL-EPIC-17 can be configured for remote access by redirecting the console to a serial communications port. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

Console redirection settings are configured in the Advanced > Remote Access Configuration menu of CMOS Setup. Console redirection is enabled by default. The decision to redirect the console is made early in BIOS execution and cannot be changed later.

Console redirection can be disabled or redirected to a different COM port. The default settings for the redirected console are 115.2 Kbps, 8 data bits, 1 stop bit, no parity, and no flow control.

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter.

System 1 Name Pin	<-->	System 2 Pin Name
TX 3	<-->	2 RX
RX 2	<-->	3 TX
RTS 7	<-->	1 DCD
CTS 8		
DSR 6	<-->	4 DTR
DCD 1	<-->	7 RTS
		8 CTS
DTR 4	<-->	6 DSR

Pins 1, 4, and 6 are shorted together on each connector. Unlisted pins have no connection.

Expansion Buses

PC/104-PLUS (PCI + ISA) AND PCI-104 (PCI ONLY)

PC/104-Plus and PCI-104 modules can be secured directly to the top of the VL-EPIC-17. Make sure to correctly configure the slot position jumpers on each PC/104-Plus module appropriately. PC/104 (ISA only) modules must not be positioned between the VL-EPIC-17 and any PC/104-Plus or PCI-104 modules in the stack.

The VL-EPIC-17 is compliant with revision 2.0 of the PC/104-Plus specification and can support four bus master capable PC/104-Plus modules.

The BIOS automatically allocates I/O and memory resources. However, manual PCI Interrupt routing is used.

PC/104 (ISA ONLY)

The VL-EPIC-17 provides full support for PC/104 (ISA only) expansion with the following exceptions:

- -5.0V power is not supplied on J14 pin B5. This pin is not connected.
- The ISA bus cannot be mastered by an external module. The VL-EPIC-17 is always the bus master. The MASTER signal on pin D17 of J14 is not connected.

Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the list above.

PC/104 I/O SUPPORT

The following I/O ranges are available on the ISA bus unless there is a device claiming the range on the LPC bus. Be sure to configure the ISA I/O ranges and the on-board serial ports in CMOS Setup to avoid conflicts with one another. (An OS will not allocate I/O in the legacy ISA range.)

- | | | |
|-----------------|-----------------|-----------------|
| ▪ 0x010 – 0x01F | ▪ 0x090 – 0x091 | ▪ 0x3CD |
| ▪ 0x024 – 0x02D | ▪ 0x093 – 0x097 | ▪ 0x3D0 – 0x3D3 |
| ▪ 0x030 – 0x03F | ▪ 0x09D | ▪ 0x3D6 – 0x3D9 |
| ▪ 0x044 – 0x047 | ▪ 0x0A2 – 0x0BF | ▪ 0x3DB – 0x3F5 |
| ▪ 0x04C – 0x05F | ▪ 0x0E0 – 0x16F | ▪ 0x3F7 – 0x47F |
| ▪ 0x065 | ▪ 0x178 – 0x1CF | ▪ 0x490 – 0x4CF |
| ▪ 0x06E – 0x070 | ▪ 0x1F8 – 0x375 | ▪ 0x4D2 – 0xCFB |
| ▪ 0x076 – 0x077 | ▪ 0x377 – 0x3BF | ▪ 0xD00 |
| ▪ 0x07D – 0x07F | ▪ 0x3CB | |

Available base I/O addresses for COM ports are: 010h, 2E8h, 2F8h, 3E8h, 3F8h.

PC/104 MEMORY SUPPORT

The following memory addresses are available on the ISA bus:

- A0000 – B7FFF
- D0000 – DFFFF

PC/104 IRQ SUPPORT

The following IRQs are available on the ISA bus:

- IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15

Each of the IRQs must be enabled in CMOS Setup before it can be used on the ISA bus. Because ISA IRQ sharing is not supported, make sure that any IRQ channel used for an ISA device is not used elsewhere. For example, if ISA IRQ 4 is enabled, you must use a different IRQ for COM1. IRQs may not be available to the ISA bus due to operating system limitations.

Note Some IRQs may already be assigned to on-board devices. Check the Interrupt Configuration table on page 66 to avoid conflicts.

Ethernet Interface

The first Ethernet interface (J5) is based on the Ethernet controller built in to the Vortex86DX processor. The second Ethernet interface (J6) is based on a Micrel KSZ8441-PQML controller. Both interfaces provide a standard IEEE 802.3 interface for 100Base-TX and 10Base-T applications.

ETHERNET CONNECTOR

One or two board-mounted RJ45 connectors (J5 and J6) are provided to make connection with a Category 5 or 6 Ethernet cable. The Ethernet controller auto-negotiates connection speed. The interface uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Note Custom models VL-EPIC-17EC and VL-EPIC-17ED use ruggedized latching Ethernet connectors at locations J2 (Ethernet 0) and J3 (Ethernet 1).

STATUS LED

A two-colored LED is located next to each RJ45 connector. The LEDs indicate Ethernet status as shown in the following table.

Table 6: Ethernet Status LEDs

LED	State	Description
Green (Link/Activity)	On	Active Ethernet cable plugged into RJ45 connector. No Tx/Rx data activity.
	Off	Cable not plugged into RJ45 connector. Cable not plugged into an active hub.
	Blinking	Active Ethernet cable plugged into RJ45 connector. Tx or Rx data activity detected on the cable.
Yellow (Speed)	On	100BaseTX (fast) detected on Ethernet cable.
	Off	10BaseT (slow) detected on Ethernet cable.

IDE/PATA Interface

The IDE interface is available to connect up to two IDE devices, such as hard disks or CD-ROM drives. Connector J10 is the IDE controller with a 44-pin 2 mm connector. Use CMOS Setup to specify the drive parameters of the drive.

Cable length must be 18" or less to maintain proper signal integrity.

This interface supplies power to 2.5" IDE drives. If you are connecting a 3.5" drive to the interface (using the VL-CBR-4405 44-pin to 40-pin IDE adapter), you must supply external power to the drive. The power cable attached to a 3.5" drive must be properly grounded so that motor current is not returned via the grounds in the data cable.

Table 7: J10 IDE Hard Drive Connector Pinout

Pin	Signal Name	Function	Pin	Signal Name	Function
1	Reset-	Reset signal from CPU	23	DIOW	I/O write
2	Ground	Ground	24	Ground	Ground
3	DD7	Data bus bit 7	25	DIOR	I/O read
4	DD8	Data bus bit 8	26	Ground	Ground
5	DD6	Data bus bit 6	27	IORDY	I/O ready
6	DD9	Data bus bit 9	28	CSEL	Cable select
7	DD5	Data bus bit 5	29	DMACK-	DMA acknowledge
8	DD10	Data bus bit 10	30	Ground	Ground
9	DD4	Data bus bit 4	31	INTRQ	Interrupt request
10	DD11	Data bus bit 11	32	NC	No connection
11	DD3	Data bus bit 3	33	DA1	Device address bit 1
12	DD12	Data bus bit 12	34	CBLID-	Cable type identifier
13	DD2	Data bus bit 2	35	DA0	Device address bit 0
14	DD13	Data bus bit 13	36	DA2	Device address bit 2
15	DD1	Data bus bit 1	37	CS0	Chip select 0
16	DD14	Data bus bit 14	38	CS1	Chip select 1
17	DD0	Data bus bit 0	39	DASP-	LED
18	DD15	Data bus bit 15	40	Ground	Ground
19	Ground	Ground	41	Power	+5.0 V
20	NC	Key	42	Power	+5.0 V
21	PDMARQ	DMA request	43	Ground	Ground
22	Ground	Ground	44	NC	No connection

Flash Interface

COMPACTFLASH

Connector J12 provides a socket for a Type I or Type II CompactFlash (CF) module. This IDE-based interface operates on the same channel as the IDE interface at connector J6. The CF interface supports operation in DMA mode.

The following CF modules have been tested and qualified as bootable devices by VersaLogic. Part numbers with a suffix of -3500 and -4352 are RoHS compliant.

Table 8. Qualified Bootable CF Modules

Manufacturer	Density	Mfg Part Number
Hagiwara	1 GB	CF1-1GMDG(H00AA)
Hagiwara	512 MB	CF1-512MDG(H00AA)
Silicon Systems	256 MB	SSD-C25M-3012, -3500, -4352
Silicon Systems	256 MB	SSD-C25MI-3012, -3500, -4352
Silicon Systems	512 MB	SSD-C51M-3012, -3500, -4352
Silicon Systems	512 MB	SSD-C51MI-3012, -3500, -4352
Silicon Systems	1 GB	SSD-C01G-3012, -3500, -4352
Silicon Systems	2 GB	SSD-C02G-3012, -3500, -4352
Silicon Systems	2 GB	SSD-C02GI-3012, -3500, -4352
Silicon Systems	4 GB	SSD-C04GI-3012, -3500, -4352

After installing the OS, you may configure the CF to be the first boot device, which will reduce boot time.

EUSB INTERFACE

The VL-EPIC-17EA includes an eUSB interface, as shown below. The VersaLogic VL-F15 Series of eUSB SSD modules are available in sizes of 2 GB or 4 GB. Contact [VersaLogic Sales](#) to order. eUSB modules are secured to the board using the VL-HDW-109 hardware kit from VersaLogic. The kit contains one M2.5 x 6 mm round aluminum standoff and two M2.5 x 4 mm pan head Philips screws.

Table 9: eUSB Interface Locations

J24 Pin	Signal Name	Function
1	+5V	Protected Power Supply
2	NC	Not connected
3	D-	Data –
4	NC	Not connected
5	D+	Data +
6	NC	Not connected
7	GND	Ground
8	NC	Not connected
9	Key	Physical key
10	LED	SSD LED

USB Interface

The VL-EPIC-17 provides three (EA) or four (EB) Type A USB host connectors.

Each USB port power switch (supplying +5V to the USB port) has a low-true status output that when low indicates an over-current, under-voltage, or over-temperature fault condition. This status signal for USB0 goes to bit 0 of GPIO PORT0 on the Vortex processor, and the status signal for USB1 goes to bit 1 of GPIO PORT0. You can read these GPIO ports for the status of these signals. You can also set up interrupts in the Vortex processor that can be routed to an IRQ by setting up the GPIO PORT0 interrupt control registers.

Serial Ports

The VL-EPIC-17 features four on-board 16550-based serial communications channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2 Kbps) serial ports. IRQ lines are chosen in CMOS Setup. COM ports can share interrupts with other COM ports, but not with other devices.

COM3 and COM4 can be operated in RS-232 4-wire, RS-422, or RS-485 modes. IRQ lines are chosen in the CMOS Setup.

Each COM port can be independently enabled, disabled, or assigned a different I/O base address in CMOS Setup.

COM PORT CONFIGURATION

There are no configuration jumpers for COM1 and COM2 since they only operate in RS-232 mode. Use CMOS Setup to select between RS-232 and RS-422/485 operating modes for COM3 and COM4.

Jumper block V2 is used to configure COM3 and COM4 for RS-422/485 operation. See “Jumper Summary” for details. The termination resistor should be enabled for RS-422 and the RS-485 endpoint stations. It should be disabled for RS-232 and RS-485 intermediate stations.

If RS-485 mode is used, the differential twisted pair (TxD+/RxD+ and TxD-/RxD-) is formed by connecting both transmit and receive pairs together. For example, on CBR-5009 connectors J6 and J5, the TxD+/RxD+ signal is formed by connecting pins 3 and 5, and the TxD-/RxD- signal is formed by connecting pins 2 and 4.

RS-232 mode for COM3 and COM4 is set in CMOS Setup.

COM3 / COM4 RS-485 MODE LINE DRIVER CONTROL

The TxD+/TxD- differential line driver can be turned on and off by manipulating the RTS handshaking line.

The following code example shows how to turn the line driver for COM3 on and off:

```

mov    dx,03ECh    ; Point to COM3 Modem Control register
in     al,dx      ; Fetch existing value
and    al,FDh     ; Clear bit D1
out    dx,al      ; Set RTS output High (enables line driver)

in     al,dx      ; Fetch existing value
or     al,02h     ; Set bit D1
out    dx,al      ; Set RTS output Low (disables line driver)

```

SERIAL PORT CONNECTORS

See the *Connector Location Diagrams* on page 27 for connector and cable information. The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout board VL-CBR-5009.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 11: COM1-2 Pinout – VL-CBR-5009 Connector J3

COM1	COM2	
Top DB9 J3 Pin	Bottom DB9 J3 Pin	RS-232
1	10	DCD
2	11	RXD*
3	12	TXD*
4	13	DTR
5	14	Ground
6	15	DSR
7	16	RTS
8	17	CTS
9	18	RI

Table 12: COM3-4 Pinout – VL-CBR-5009 Connectors J5-6

COM3	COM4			
J6 Pin	J5 Pin	RS-232	RS-422	RS-485
1	1	Ground	Ground	Ground
2	2	RXD	RxD-	RxD-
3	3	CTS	RxD+	RxD+
4	4	TXD	TxD-	TxD-
5	5	RTS	TxD+	TxD+

PS/2 Keyboard and Mouse

A standard PS/2 keyboard and mouse interface is accessible through connector J4 of the VersaLogic's VL-CBR-5009 breakout board. The breakout board is connected to connector J11 of the VL-EPIC-17. The +5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 13: PS/2 Mouse and Keyboard Pinout

VL-CBR-5009 J4 Top	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	MSCLK	Mouse Clock
6	–	No Connection
VL-CBR-5009 J4 Bottom	Signal	Description
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	KBCLK	Keyboard Clock
6	–	No Connection

Pushbutton Reset

Connector J11 includes an input for a pushbutton reset switch. Shorting J11 pin 37 to ground causes the VL-EPIC-17 to reboot. This must be a mechanical switch or an open-collector or open-drain active switch with less than a 0.5V low-level input when the current is 1 mA. There must be no pull-up resistor on this signal.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the VL-CBR-5009 breakout board.

External Speaker

A miniature 8 ohm speaker can be connected between J11 pin 50 (SPKO*) and J11 pin 49. A speaker is provided on the VL-CBR-5009 breakout board.

Programmable LED

Connector J11 includes an output signal for attaching a software-controlled LED. Connect the cathode of the LED to J11 pin 48; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the VL-CBR-5009 breakout board.

To turn the LED on and off, set or clear bit D11 in I/O port 1E0h. When changing the register, make sure not to alter the values of the other bits. The following code examples show how to turn the LED on and off:

LED On		LED Off	
mov	dx, 1E0h	mov	dx, 1E0h
in	al, dx	in	al, dx
or	al, 80h	and	al, 7fh
out	dx, al	out	dx, al

Note The LED is turned on by the BIOS during system startup (about 10 seconds after power up). This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

Digital I/O

The 40-pin I/O connector (J9) incorporates 32 digital I/O lines. Table 14 shows the function of each pin. The digital I/O lines are controlled using the SPI registers. See "SPI Registers" for a complete description of the registers.

The digital lines are grouped into two banks of 16-bit bi-directional ports. The direction of each 8-bit port is controlled by software. The digital I/O lines are powered up in the input mode. The 24 mA source/sink drive and short protected outputs are an excellent choice for industrial LVTTL interfacing. All I/O pins use +3.3V signaling.

Warning! Damage may occur if the I/O pins are connected to +5V logic.

Table 14: J9 I/O Connector Pinout

J9 Pin	Signal	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Label)
1	Digital I/O 1	J1	5 (IO1)
2	Digital I/O 2		4 (IO2)
3	Digital I/O 3		3 (IO3)
4	Digital I/O 4		2 (IO4)
5	Ground		1 (GND1)
6	Digital I/O 5	J2	5 (IO5)
7	Digital I/O 6		4 (IO6)
8	Digital I/O 7		3 (IO7)
9	Digital I/O 8		2 (IO8)
10	Ground		1 (GND1)
11	Digital I/O 9	J3	5 (IO9)
12	Digital I/O 10		4 (IO10)
13	Digital I/O 11		3 (IO11)
14	Digital I/O 12		2 (IO12)
15	Ground		1 (GND2)
16	Digital I/O 13	J4	5 (IO13)
17	Digital I/O 14		4 (IO14)
18	Digital I/O 15		3 (IO15)
19	Digital I/O 16		2 (IO16)
20	Ground		1 (GND2)
21	Digital I/O 17	J6	1 (IO17)
22	Digital I/O 18		2 (IO18)
23	Digital I/O 19		3 (IO19)
24	Digital I/O 20		4 (IO20)
25	Ground		5 (GND3/PBRST#)
26	Digital I/O 21	J7	1 (IO21)
27	Digital I/O 22		2 (IO22)
28	Digital I/O 23		3 (IO23)
29	Digital I/O 24		4 (IO24)
30	Ground		5 (GND3)
31	Digital I/O 25	J8	1 (IO25)
32	Digital I/O 26		2 (IO26)
33	Digital I/O 27		3 (IO27)
34	Digital I/O 28		4 (IO28)
35	Ground		5 (GND4)
36	Digital I/O 29	J9	1 (IO29)
37	Digital I/O 30		2 (IO30)
38	Digital I/O 31		3 (IO31)
39	Digital I/O 32		4 (IO32)
40	Ground		5 (GND4)

DIGITAL I/O PORT CONFIGURATION USING THE SPI INTERFACE

Digital I/O channels 0-31 are accessed via SPI slave select 6 (writing 6h to the SS field in SPICONTROL). Each pair of I/O ports is configured by a set of paged I/O registers accessible through SPI. These registers control settings such as signal direction, input polarity, and interrupt source.

Digital I/O Initialization Using the SPI Interface

There are two Microchip MCP23S17 digital I/O devices used. Digital I/O channels 0-15 map to device #0 (address “000”) and channels 15-31 to device #1 (address “001”). Please refer to the [Microchip MCP23S17 datasheet](#) for more information about the MCP23S17. Before accessing the digital I/O devices a ‘1’ must be written to the control bit HAEN in the IOCON register (write a 8h to this register) in the MCP23S17 devices. This write is done to device address “000” which will actually write this HAEN bit to both devices. Once this HAEN bit is set, both devices can be independently accessed. This must be done anytime these parts are reset. Example code is shown below (this assumes the FPGA base address is the default setting CA0h).

```

MOV    DX, 1Eh
MOV    AL, 26h        ;SPICONTROL: SPI Mode 00, 24bit, auto, SPI 6
OUT    DX, AL
MOV    DX, 1E9h
MOV    AL, 30h        ;SPISTATUS: 8 MHz, no IRQ, left-shift
OUT    DX, AL
MOV    DX, 1EBh
MOV    AL, 08h        ;SPIDATA1: Set HAEN Bit to a '1'
OUT    DX, AL
MOV    DX, 1ECh
MOV    AL, 0Ah        ;SPIDATA2: MCP23S17 IOCON addr 0x0A
OUT    DX, AL
MOV    DX, 1EDh
MOV    AL, 40h        ;SPIDATA3: MCP23S17 write to device "000"
OUT    DX, AL

BUSY:  MOV    DX, 1E9h
        IN     AL, DX        ;Get SPI status
        AND    AL, 01h      ;Isolate the BUSY bit
        JNZ   BUSY         ;Loop back if SPI transaction is not complete

```

Digital I/O Interrupt Generation Using the SPI Interface

Digital I/O can be configured to issue hardware interrupts on the transition (high to low or low to high) of any digital I/O pin. IRQ assignment is made in SPI control register SPISTATUS. This IRQ is shared among all SPI devices connected to the VL-EPIC-17 (the ADC and DAC devices on the SPI interface do not have interrupts). Digital I/O chip interrupt configuration is achieved through I/O port register settings. Please refer to the [Microchip MCP23S17 datasheet](#) for more information.

The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts. The following code example illustrates how to do this for device #0 on channels 0-15. Normally, the BIOS initializes the on-board digital I/O chips at boot time.

```

MOV    DX, 1E8h
MOV    AL, 26h      ;SPICONTROL: SPI Mode 00, 24bit, auto SPI 6
OUT    DX, AL
MOV    DX, 1E9h
MOV    AL, 30h     ;SPISTATUS: 8 MHz, no IRQ, left-shift
OUT    DX, AL
MOV    DX, 1EBh
MOV    AL, 44h     ;SPIDATA1: Mirror & Open-Drain interrupts
OUT    DX, AL
MOV    DX, 1ECh
MOV    AL, 0Ah     ;SPIDATA2: MCP23S17 address 0x0A
OUT    DX, AL
MOV    DX, 1EDh
MOV    AL, 40h     ;SPIDATA3: MCP23S17 write command
OUT    DX, AL

BUSY:  MOV    DX, 1E9h
        IN     AL, DX      ;Get SPI status
        AND    AL, 01h     ;Isolate the BUSY bit
        JNZ   BUSY        ;Loop back if SPI transaction is not complete

MOV    DX, 1E8h
MOV    AL, 27h     ;SPICONTROL: SPI Mode 00, 24bit, auto SPI 6
OUT    DX, AL
MOV    DX, 1E9h
MOV    AL, 30h     ;SPISTATUS: 8 MHz, no IRQ, left-shift
OUT    DX, AL
MOV    DX, 1EBh
MOV    AL, 44h     ;SPIDATA1: Mirror & Open-Drain interrupts
OUT    DX, AL
MOV    DX, 1ECh
MOV    AL, 0Ah     ;SPIDATA2: MCP23S17 address 0x0A
OUT    DX, AL
MOV    DX, 1EDh
MOV    AL, 40h     ;SPIDATA3: MCP23S17 write command
OUT    DX, AL

```

Writing to a Digital I/O Port Using the SPI Interface

The following code example initiates a write of 55h to Digital I/O port bits DIO15-DIO8.

```

;Write 44h to configure MCP23S17 register IOCON

MOV    DX, 1E8h
MOV    AL, 26h     ;SPICONTROL: SPI Mode 00, 24bit, SPI 6
OUT    DX, AL
MOV    DX, 1E9h
MOV    AL, 30h     ;SPISTATUS: 8 MHz, no IRQ, left-shift
OUT    DX, AL
MOV    DX, 1EBh
MOV    AL, 44h     ;SPIDATA1: mirror and open-drain interrupts
OUT    DX, AL
MOV    DX, 1ECh
MOV    AL, 0Ah     ;SPIDATA2: MCP23S17 IOCON register address 0Ah
OUT    DX, AL
MOV    DX, 1EDh
MOV    AL, 40h     ;SPIDATA3: MCP23S17 write command
OUT    DX, AL
CALL   BUSY        ;Poll busy flag to wait for SPI transaction

```

```

;Configure MCP23S17 register IODIRA for outputs

MOV    DX, 1EBh
MOV    AL, 00h      ;SPIDATA1: 00h for outputs
OUT    DX, AL
MOV    DX, 1ECh
MOV    AL, 00h      ;SPIDATA2: MCP23S17 register address 00h
OUT    DX, AL
MOV    DX, 1EDh
MOV    AL, 40h      ;SPIDATA3: MCP23S17 write command
OUT    DX, AL
CALL   BUSY        ;Poll busy flag to wait for SPI transaction

;Write 55h to MCP23S17 register GPIOA

MOV    DX, 1EBh
MOV    AL, 55h      ;SPIDATA1: data to write
OUT    DX, AL
MOV    DX, 1ECh
MOV    AL, 14h      ;SPIDATA2: MCP23S17 register address 14h
OUT    DX, AL
MOV    DX, 1EDh
MOV    AL, 40h      ;SPIDATA3: MCP23S17 write command
OUT    DX, AL
CALL   BUSY        ;Poll busy flag to wait for SPI transaction

BUSY:  MOV    DX, 1E9h
        IN    AL, DX      ;Get SPISTATUS
        AND   AL, 01h     ;Isolate the BUSY flag
        JNZ   BUSY       ;Loop if SPI transaction not complete

```

Reading a Digital I/O Port Using the SPI Interface

The following code example reads the DIO15-DIO8 input lines.

```
'REGISTER ASSIGNMENT
'-----
CONST SPICONTROL1 = &H1E8
CONST SPICONTROL2 = &H1E9
CONST SPISTATUS = &H1E9
CONST SPIDATA1 = &H1EB
CONST SPIDATA2 = &H1EC
CONST SPIDATA3 = &H1ED

'INITIALIZE SPI CONTROLLER
'=====

'SPICONTROL1 Register
'-----
'D7 CPOL      = 0 SPI Clock Polarity (SCLK idles low)
'D6 CPHA      = 0 SPI Clock Phase (Data read on rising edge)
'D5 SPILEN1   = 1 SPI Frame Length (24-Bit)
'D4 SPILEN0   = 0 " " " "
'D3 MAN_SS    = 0 SPI Slave Select Mode (Automatic)
'D2 SS2       = 1 SPI Slave Select (On-Board DIO 0-15)
'D1 SS1       = 1 " " " "
'D0 SS0       = 0 " " " "
OUT SPICONTROL1, &H26

'SPICONTROL2 Register
'-----
'D7 IRQSEL1   = 0 IRQ Select (IRQ3)
'D6 IRQSEL0   = 0 " " "
'D5 SPICLK1   = 1 SPI SCLK Frequency (8.333 MHz)
'D4 SPICLK0   = 1 " " "
'D3 HW_IRQ_EN = 0 Hardware IRQ Enable (Disabled)
'D2 LSBIT_1ST = 0 SPI Shift Direction (Left Shifted)
'D1 0         = 0 This bit has no function
'D0 0         = 0 This bit has no function
OUT SPICONTROL2, &H30

'INITIALIZE MCP23S17
'=====

'MCP23S17 IOCON Register
'-----
'D7 BANK      = 0 Registers in same bank (addresses are sequential)
'D6 MIRROR    = 1 The INT pins are internally connected
'D5 SEQOP     = 0 Sequential op disabled. Addr ptr does not increment.
'D4 DISSLW    = 0 Slew rate control for SDA output (enabled)
'D3 HAEN      = 0 Hardware address enable (addr pins disabled)
'D2 ODR       = 1 INT pin is open-drain
'D1 INTPOL    = 0 Polarity of INT output pin (ignored when ODR=1)
'D0 0         = 0 This bit has no function
OUT SPIDATA1, &H44

'MCP23S17 IOCON Register Address
'-----
OUT SPIDATA2, &HA

'MCP23S17 SPI Control Byte (Write)
'-----
'D7 SLAVEFA3  = 0 Slave Address (Fixed Portion)
'D6 SLAVEFA2  = 1 " " "
'D5 SLAVEFA1  = 0 " " "
'D4 SLAVEFA0  = 0 " " "
'D3 SLAVEHA2  = 0 Slave Address Bits (Hardware Address Bits)
```

```

'D2 SLAVEHA1 = 0 " " " "
'D1 SLAVEHA0 = 0 " " " "
'D0 READWRITE = 0 Read/Write Bit = Write
OUT SPIDATA3, &H40

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'INITIALIZE DIRECTION OF DIO LINES D15-D8 AS INPUTS
'=====

'Direction = All Inputs
OUT SPIDATA1, &HFF

'MCP23S17 IODIRA Register Address
OUT SPIDATA2, &H0

'MCP23S17 SPI Control Byte (Write)
OUT SPIDATA3, &H40

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'Repeat until ESC key is pressed
WHILE INKEY$ <> CHR$(27)

'READ DIO INPUT DATA FROM MCP23S17
'-----

'MCP23S17 GPIOA Register Address
OUT SPIDATA2, &H12

'MCP23S17 SPI Control Byte (Read)
OUT SPIDATA3, &H41

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'DIO Input Data
PRINT HEX$(INP(SPIDATA1))

WEND

SYSTEM

```

Analog Input

The VL-EPIC-17 employs a multi-range, 12-bit A/D converter that accepts up to eight (EA) or sixteen (EB) single-ended input signals. The converter features 500K samples per second, with an input range of 0 to +4.095V.

The A/D converter is accessed through the SPI interface.

SOFTWARE CONFIGURATION

Configure the SPX registers for Analog Input. The VL-EPIC-17 cannot be configured to issue an interrupt upon completion of an A/D conversion, so the software must poll the BUSY bit to determine when the conversion is complete.

EXTERNAL CONNECTIONS

Single-ended analog voltages are applied to connectors J1 and J2 of the VL-CBR-4004 board (connected to J18 of the VL-EPIC-17) as shown in the following table.

Table 15: Analog Input Connector

J18 Pin	Signal	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Label)
1	Analog Input 1	J1 Analog Input	5 (IO1)
2	Analog Input 2		4 (IO2)
3	Analog Input 3		3 (IO3)
4	Analog Input 4		2 (IO4)
5	Ground		1 (GND1)
6	Analog Input 5	J2 Analog Input	5 (IO5)
7	Analog Input 6		4 (IO6)
8	Analog Input 7		3 (IO7)
9	Analog Input 8		2 (IO8)
10	Ground		1 (GND1)
11	Analog Input 9	J3 Analog Input (EB)	5 (IO9)
12	Analog Input 10		4 (IO10)
13	Analog Input 11		3 (IO11)
14	Analog Input 12		2 (IO12)
15	Ground		1 (GND2)
16	Analog Input 13	J4 Analog Input (EB)	5 (IO13)
17	Analog Input 14		4 (IO14)
18	Analog Input 15		3 (IO15)
19	Analog Input 16		2 (IO16)
20	Ground		1 (GND2)

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

INITIATING AN ANALOG CONVERSION

The following procedure can be used to initiate an analog conversion.

1. Write 15h to the SPICONTROL register (I/O address 1E8h) – This value configures the SPI port to select the on-board A/D converter, 16-bit frame length, low SCLK idle state, rising edge SCLK edge, and automatic slave select.
2. Write 30h to the SPISTATUS register (I/O address 1E9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.
3. Write any value to SPIDATA2 (I/O address 1ECh) – This data will be ignored by the A/D converter.
4. Write the analog input channel number to bits 5-3 of SPIDATA3 (1EDh) – Any write operation to this register triggers an SPI transaction.
5. Poll the BUSY bit in bit 0 of SPISTATUS register (I/O address 1E9h) until the conversion is completed.
6. Read the conversion data from SPIDATA2 (lower 8 bits) and SPIDATA3 (upper 4 bits).

Each analog conversion returns the conversion data from the previous conversion. The first analog conversion after power-up or reset returns the data from ADCH0. The second conversion returns the conversion data from the channel addressed in the first conversion. Each successive conversion returns conversion data from the previous conversion.

This means that multiple conversions on the same A/D channel return valid data after every conversion, starting with the second conversion. However, if a different channel is selected between analog reads, two conversions will be necessary to return valid data from the new channel. The analog input code example on page 50 shows how to use a 32-bit SPI frame for an automatic second conversion when only one sample is desired.

ANALOG INPUT RANGE

Analog inputs are in binary format, 0 to +4.095V only.

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 Volts (ground). All codes are considered positive.

Sample values are shown in the following table:

Table 16: Binary Data Format

0 to +5V Input Voltage	Hex	Decimal	Comment
>+4.095	–	–	Out of range
+4.095	0FFFh	4095	Maximum voltage
+2.047	0800h	2048	Half scale
+1.023	0400h	1024	Quarter scale
+0.001	0001h	1	1 LSB
0.000	0000h	0	Zero (ground input)

ANALOG INPUT CODE EXAMPLE

The following code example illustrates the procedure for reading an analog voltage from the onboard ADC channel 3. A 32-bit SPI frame is used to provide a valid single sample.

```

MOV     DX, 1E8h
MOV     AL, 35h           ;SPICONTROL: SPI Mode 00, 32-bit,
                        ;auto ADC_SS#

OUT     DX, AL
MOV     DX, 1E9h
MOV     AL, 30h           ;SPISTATUS: 8 MHz, no IRQ, left-shift
OUT     DX, AL

                        ;SPIDATA2, SPIDATA1, SPIDATA0: don't care

MOV     DX, 1EDh
MOV     AL, 18h           ;SPIDATA3: ADC78H90 AIN4 = EBX-11 ADCH3
OUT     DX, AL

BUSY:   MOV     DX, 1E9h   ;Get SPISTATUS
        IN      AL, DX
        AND     AL, 01h   ;Isolate the BUSY bit
        JNZ     BUSY     ;Loop back if SPI transaction not complete

        MOV     DX, 1EAh   ;Point to SPIDATA0 register
        IN      AX, DX     ;16-bit input reads current conversion data
                        ;from SPIDATA1 into AH and from SPIDATA0 into
                        ;AL

```

For more detailed information on the VL-EPIC-17 A/D converter, please refer to the [National Semiconductor ADC78H90 Datasheet](#).

Analog Output

The VL-EPIC-17 provides a four (EA) or eight (EB) channel 12-bit, unipolar digital-to-analog converter (DAC). The converter has 5 μ s per-channel update rate with a 0 to +4.096V output voltage range.

The VL-EPIC-17 DAC is controlled using the SPI registers. The DAC is accessed via SPI slave select 7 (writing 7h to the SS field in SPICONTROL). See "SPI Registers" for a complete description of the registers.

See the [National Semiconductor DAC124S085 Datasheet](#) for programming information.

Table 17: Analog Output Pinout

J18 Pin	Signal	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Label)
21	Analog Output 1	J6 Analog Output	1 (IO17)
22	Analog Output 2		2 (IO18)
23	Analog Output 3		3 (IO19)
24	Analog Output 4		4 (IO20)
25	Ground		5 (GND3/PBRST#)
26	Analog Output 5	J7 Analog Output (EB)	1 (IO21)
27	Analog Output 6		2 (IO22)
28	Analog Output 7		3 (IO23)
29	Analog Output 8		4 (IO24)
30	Ground		5 (GND3)

Analog Output Using the SPI Interface

The following procedure can be used to set an analog output using the SPI interface.

1. Write 17h to the SPICONTROL register (I/O address 1E8h) – This value configures the SPI port to select the DAC, 16-bit frame length, low SCLK idle state, rising edge SCLK edge, and automatic slave select.
2. Write 30h to the SPISTATUS register (I/O address 1E9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.
3. Write the LS 8-bits of the 12-bit output value to SPIDATA2 (I/O address 1ECh). For example, if writing a 12-bit value of 123h the value of 23h is written to SPIDATA2.
4. Write the analog output channel number (0 to 3) to Bits 7-6 and the “write to specific register and update outputs” 1h to Bits 5-4 and the LS 4-bits of the 12-bit output value to SPIDATA3 (I/O address 1EDh) – Any write operation to this register address triggers an SPI transaction. For example, if writing to the third DAC channel (channel number 2) with a 12-bit output value of 123h then the value written to SPIDATA3 is 91h. Note: Nothing has to be written to, or read from, SPIDATA1 or SPIDATA0.
5. Poll the SPI BUSY bit in the SPISTATUS register (I/O address 1E9h) until the conversion is completed.
6. The D/A output will be stable in no more than 5 μ s.

Counter/Timers

The VL-EPIC-17 includes three uncommitted 8254 type counter/timer channels for general program use. External control signals for the three channels are available on connector J18 (see Table 18).

Table 18: J22 Counter Timer Pinout

J18 Pin	Signal Direction*	Signal Name	Function	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Label)
31	Output	OCTC3	Timer 3 Counter Output	J8	1 (IO25)
32	Input	GCTC3	Timer 3 Gate Input		2 (IO26)
33	Input	ICTC3	Timer 3 Clock Input		3 (IO27)
34	Output	OCTC4	Timer 4 Counter Output		4 (IO28)
36	Input	GCTC4	Timer 4 Gate Input	J9	1 (IO29)
37	Input	ICTC4	Timer 4 Clock Input		2 (IO30)
38	Output	OCTC5	Timer 5 Counter Output		3 (IO31)
39	Input	GCTC5	Timer 5 Gate Input		4 (IO32)

* Relative to VL-EBX-37

The Custom Programming appendix discusses how to use and configure these timers using the following registers.

Register	Read/Write	Address	Name
IRQCTRL	R/W	1E3h	Interrupt Control Register
IRQSTAT	R-Status/Write-Clear	1E4h	Interrupt Status Register
TMCNTRL	R/W	1E5h	Timer Control Register
TIMBASEMS	R/W	1E6h	Timer Base MS Address Register
TIMBASELS	R/W	1E6h	Timer Base LS Address Register

SPX

Up to four serial peripheral expansion (SPX) devices can be attached to the VL-EPIC-17 at connector J13 using the VL-CBR-1401 or VL-CBR-1402 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: SCLK, MISO, and MOSI, as well as four chip selects, SS0# to SS3#, and an interrupt input, SINT#.

The +5V power provided to pins 1 and 14 of J13 is protected by a 1 Amp resettable fuse.

Table 19: SPX Expansion Bus Pinout

J13 Pin	Signal Name	Function
1	V5_0	+5V (Protected)
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Serial Data In
5	GND	Ground
6	MOSI	Serial Data Out
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1
10	SS2#	Chip Select 2
11	SS3#	Chip Select 3
12	GND	Ground
13	SINT#	Interrupt Input
14	V5_0	+5V (Protected)

SPI is, in its simplest form, a three-wire serial bus. One signal is a Clock, driven only by the permanent Master device on-board. The others are Data In and Data Out with respect to the Master. The SPX implementation adds additional features, such as chip selects and an interrupt input to the Master. The Master device initiates all SPI transactions. A slave device responds when its Chip Select is asserted and it receives Clock pulses from the Master.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. Please note that since this clock is divided from a 33 MHz PCI clock, the actual generated frequencies are not discrete integer MHz frequencies. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

VERSALOGIC SPX EXPANSION MODULES

VersaLogic offers a number of SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2" x 3.78") that can mount on the PC/104 stack using standard standoffs, or up to two feet away from the baseboard. For more information, contact VersaLogic at Info@VersaLogic.com.

SPI REGISTERS

A set of control and data registers are available for SPI transactions. The following tables describe the SPI control registers (SPICONTROL and SPISTATUS) and data registers (SPIDATA3-0).

SPICONTROL (READ/WRITE) 1E8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 20: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description																																																								
D7	CPOL	SPI Clock Polarity – Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high																																																								
D6	CPHA	SPI Clock Phase – Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge																																																								
D5-D4	SPILEN	SPI Frame Length – Sets the SPI frame length. This selection works in manual and auto slave select modes. <table border="1"> <thead> <tr> <th>SPILEN1</th> <th>SPILEN0</th> <th>Frame Length</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>8-bit</td> </tr> <tr> <td>0</td> <td>1</td> <td>16-bit</td> </tr> <tr> <td>1</td> <td>0</td> <td>24-bit</td> </tr> <tr> <td>1</td> <td>1</td> <td>32-bit</td> </tr> </tbody> </table>	SPILEN1	SPILEN0	Frame Length	0	0	8-bit	0	1	16-bit	1	0	24-bit	1	1	32-bit																																									
SPILEN1	SPILEN0	Frame Length																																																								
0	0	8-bit																																																								
0	1	16-bit																																																								
1	0	24-bit																																																								
1	1	32-bit																																																								
D3	MAN_SS	SPI Manual Slave Select Mode – This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1EDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual																																																								
D2-D0	SS	SPI Slave Select – These bits select which slave select will be asserted. The SSx# pin on the baseboard will be directly controlled by these bits when MAN_SS = 1. The following is the default definition (ADIOMODE = 0): <table border="1"> <thead> <tr> <th>SS2</th> <th>SS1</th> <th>SS0</th> <th>Slave Select</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>None, port disabled</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>SPX Slave Select 0, J23 pin-8</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>SPX Slave Select 1, J23 pin-9</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>SPX Slave Select 2, J23 pin-10</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>SPX Slave Select 3, J23 pin-11</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>A/D Converter Channels 1-8 (on-board)</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Digital I/O (on-board)</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>D/A Converter Channels 1-4 (on-board)</td> </tr> </tbody> </table> The following are the definitions when ADIOMODE = 1. The ADIOMODE bit is defined in Bit 0 of Register 1EEd below. <table border="1"> <thead> <tr> <th>SS2</th> <th>SS1</th> <th>SS0</th> <th>Slave Select</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>None, port disabled</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>SPX Slave Select 0, J23 pin-8</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>SPX Slave Select 1, J23 pin-9</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>A/D Converter Channels 9-16 (on-board)</td> </tr> </tbody> </table>	SS2	SS1	SS0	Slave Select	0	0	0	None, port disabled	0	0	1	SPX Slave Select 0, J23 pin-8	0	1	0	SPX Slave Select 1, J23 pin-9	0	1	1	SPX Slave Select 2, J23 pin-10	1	0	0	SPX Slave Select 3, J23 pin-11	1	0	1	A/D Converter Channels 1-8 (on-board)	1	1	0	Digital I/O (on-board)	1	1	1	D/A Converter Channels 1-4 (on-board)	SS2	SS1	SS0	Slave Select	0	0	0	None, port disabled	0	0	1	SPX Slave Select 0, J23 pin-8	0	1	0	SPX Slave Select 1, J23 pin-9	0	1	1	A/D Converter Channels 9-16 (on-board)
SS2	SS1	SS0	Slave Select																																																							
0	0	0	None, port disabled																																																							
0	0	1	SPX Slave Select 0, J23 pin-8																																																							
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1	0	1	A/D Converter Channels 1-8 (on-board)																																																							
1	1	0	Digital I/O (on-board)																																																							
1	1	1	D/A Converter Channels 1-4 (on-board)																																																							
SS2	SS1	SS0	Slave Select																																																							
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0	1	0	SPX Slave Select 1, J23 pin-9																																																							
0	1	1	A/D Converter Channels 9-16 (on-board)																																																							

Bit	Mnemonic	Description
		1 0 0 D/A Converter Channels 5-8 (on-board)
		1 0 1 A/D Converter Channels 1-8 (on-board)
		1 1 0 Digital I/O (on-board)
		1 1 1 D/A Converter Channels 1-4 (on-board)

SPIAUX (READ/WRITE) 1EEh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ADIOMODE

Table 21: SPI Auxiliary Control Bit Assignments

Bit	Mnemonic	Description
D7-D1	Reserved	These bits are reserved and only 0 should be written to them.
D0	ADIOMODE	<p>SPI Decode Mode Select – This bit selects either the standard SPX decode or the decode to allow access to the second A/D channels 9-16 and the second D/A channels 5-8. See the SPICONTROL SPX register for its use.</p> <p>0 = Standard SPX interface decode (default)</p> <p>1 = Decode to support access to A/D channels 9-16 and D/A channels 5-8</p>

SPISTATUS (READ/WRITE) 1E9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 22: SPI Control Register 2 Bit Assignments

Bit	Mnemonic	Description															
D7-D6	IRQSEL	<p>IRQ Select – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality.</p> <table border="1"> <tr> <td>IRQSEL1</td> <td>IRQSEL0</td> <td>IRQ</td> </tr> <tr> <td>0</td> <td>0</td> <td>IRQ3</td> </tr> <tr> <td>0</td> <td>1</td> <td>IRQ4</td> </tr> <tr> <td>1</td> <td>0</td> <td>IRQ5</td> </tr> <tr> <td>1</td> <td>1</td> <td>IRQ10</td> </tr> </table>	IRQSEL1	IRQSEL0	IRQ	0	0	IRQ3	0	1	IRQ4	1	0	IRQ5	1	1	IRQ10
IRQSEL1	IRQSEL0	IRQ															
0	0	IRQ3															
0	1	IRQ4															
1	0	IRQ5															
1	1	IRQ10															
D5-D4	SPICLK	<p>SPI SCLK Frequency – These bits set the SPI clock frequency.</p> <table border="1"> <tr> <td>SPICLK1</td> <td>SPICLK0</td> <td>Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1.042 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>2.083 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>4.167 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>8.333 MHz</td> </tr> </table>	SPICLK1	SPICLK0	Frequency	0	0	1.042 MHz	0	1	2.083 MHz	1	0	4.167 MHz	1	1	8.333 MHz
SPICLK1	SPICLK0	Frequency															
0	0	1.042 MHz															
0	1	2.083 MHz															
1	0	4.167 MHz															
1	1	8.333 MHz															
D3	HW_IRQ_EN	<p>Hardware IRQ Enable – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled</p> <p>Note: The selected IRQ is shared with ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.</p>															
D2	LSBIT_1ST	<p>SPI Shift Direction – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)</p>															
D1	HW_INT	<p>SPI Device Interrupt State – This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT#</p> <p>This bit is read-only and is cleared when the SPI device's interrupt is cleared.</p>															
D0	BUSY	<p>SPI Busy Flag – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers</p> <p>This bit is read-only.</p>															

SPIDATA0 (READ/WRITE) 1EAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) 1EBh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) 1ECh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) 1EDh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit uses the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.

Data returning from the SPI target will normally have its most significant data in the SPIDATA3 register. An exception will occur when LSBIT_1ST = 1 to indicate a right-shift transaction. In this case the most significant byte of an 8-bit transaction will be located in SPIDATA0, a 16-bit transaction's most significant byte will be located in SPIDATA1, and a 24-bit transaction's most significant byte will be located in SPIDATA2.

System Resources and Maps

Memory Map

The lower 1 MB memory map of the VL-EPIC-17 is arranged as shown in the following table. Various blocks of memory space between A0000h and FFFFFh are shadowed.

Table 23: Memory Map

Start Address	End Address	Comment
F0000h	FFFFFh	System BIOS Area
E0000h	FFFFFh	Extended System BIOS Area
C0000h	DFFFFh	Expansion Area
A0000h	BFFFFh	Legacy Video Area
00000h	9FFFFh	Legacy System (DOS) Area

I/O Map

The following table lists the common I/O devices in the VL-EPIC-17 I/O map. User I/O devices should be added using care to avoid the devices already in the map as shown below.

Table 24: On-Board I/O Devices

I/O Device	Standard I/O Addresses
PLED and Product ID Register	1E0h
Revision Indicator Register	1E1h
BIOS and Jumper Status Register	1E2h
Interrupt Control Register	1E3h
Interrupt Mask Register	1E4h
Interrupt Status Register	1E5h
8254 Timer Control	1E6h
Reserved for System Test	1E7h
SPX Expansion Interface	1E8 – 1EEh
Reserved for System Test	1EFh
Reserved for Future Use	1D0 – 1DBh
8254 Timer Address 0	1DCh
8254 Timer Address 1	1DDh
8254 Timer Address 2	1DEh
8254 Timer Address 3	1DFh
Primary IDE Controller	1F0h – 1F7h
COM2 Serial Port Default	2F8h – 2FFh
COM1 Serial Port Default	3F8h – 3FFh

Interrupt Configuration

Table 25: Interrupt Configuration

● = default setting ○ = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer 0	●															
Keyboard		●														
Slave PIC			●													
COM1				○	●	○	○	○		○	○	○	○			
COM2				●	○	○	○	○		○	○	○	○			
COM3				○	○	○	○	○		○	●	○	○			
COM4				○	○	○	○	○		○	○	●	○			
Watchdog*				○	○	○	○	○		○	○	○	○			
RTC									●							
Mouse													●			
Math Chip														●		
Pri. IDE															●	
ISA IRQ3				○												
ISA IRQ4					○											
ISA IRQ5						○										
ISA IRQ6							○									
ISA IRQ7								○								
ISA IRQ9										○						
ISA IRQ10											○					
ISA IRQ11												○				
ISA IRQ12													○			
ISA IRQ15																○
PCI INTA#				○	○	○	○	○		○	○	○	○		○	○
PCI INTB#				○	○	○	○	○		○	○	○	○		○	○
PCI INTC#				○	○	○	○	○		○	○	○	○		○	○
PCI INTD#				○	○	○	○	○		○	○	○	○		○	○

* The watchdog timer can also be set to NMI. The default setting is to reset the CPU board.



PLED and Product Code Register

PLEDPC (Read/Write) 1E0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Table 26: PLED and Product Code Register Bit Assignments

Bit	Mnemonic	Description																
D7	PLED	Light Emitting Diode — Controls the programmable LED on connector J7. 0 = Turns LED off 1 = Turns LED on																
D6-D0	PC	Product Code — These bits are hard-coded to represent the product type. The VL-EPIC-17 always reads as 0000011. Other codes are reserved for future products. <table style="margin-left: auto; margin-right: auto;"> <tr> <td>PC6</td> <td>PC5</td> <td>PC4</td> <td>PC3</td> <td>PC2</td> <td>PC1</td> <td>PC0</td> <td>Product Code</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>VL-EPIC-17</td> </tr> </table> These bits are read-only.	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Product Code	0	0	0	1	0	0	1	VL-EPIC-17
PC6	PC5	PC4	PC3	PC2	PC1	PC0	Product Code											
0	0	0	1	0	0	1	VL-EPIC-17											

PLD Revision and Type Register

REVTYP (Read-Only) 1E1h

D7	D6	D5	D4	D3	D2	D1	D0
PLD4	PLD3	PLD2	PLD1	PLD0	TEMP	CUSTOM	BETA

This register is used to indicate the revision level of the VL-EPIC-17.

Table 27: Revision and Type Register Bit Assignments

Bit	Mnemonic	Description												
D7-D3	PLD	<p>PLD Code Revision Level — These bits are hard-coded and represent the PLD code revision.</p> <table> <thead> <tr> <th>PLD4</th> <th>PLD3</th> <th>PLD2</th> <th>PLD1</th> <th>PLD0</th> <th>Revision</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Rev. 1.0x</td> </tr> </tbody> </table> <p>These bits are read-only.</p>	PLD4	PLD3	PLD2	PLD1	PLD0	Revision	0	0	0	1	0	Rev. 1.0x
PLD4	PLD3	PLD2	PLD1	PLD0	Revision									
0	0	0	1	0	Rev. 1.0x									
D2	TEMP	<p>Temperature Rating — This bit indicates whether the VL-EPIC-17 is rated for standard or extended temperature operation.</p> <p>0 = Standard temperature operation 1 = Extended temperature operation</p> <p>This bit is read-only.</p>												
D1	CUSTOM	<p>PLD Class — This bit indicates whether the PLD code is standard or customized.</p> <p>0 = Standard PLD code 1 = Custom PLD code</p> <p>This bit is read-only.</p>												
D0	BETA	<p>Production Level — This bit indicates if the PLD code is at the beta or production level.</p> <p>0 = Production level PLD 1 = Beta level PLD</p> <p>This bit is read-only.</p>												

GPI Jumper Register

GPI (Read-Only) 1E2h

D7	D6	D5	D4	D3	D2	D1	D0
GPI1_JMP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPI2_JMP

Table 28: GPI Register Bit Assignments

Bit	Mnemonic	Description
D7	GPI1_JMP	General Purpose Input 1 Jumper — Indicates the status of jumper V4[1-2]. 0 = Jumper out 1 = Jumper in This bit is read-only.
D6-D1	Reserved	These bits have no function.
D0	GPI2_JMP	General Purpose Input 2 Jumper — Indicates the status of jumper V4[3-4]. 0 = Jumper out 1 = Jumper in This bit is read-only.

Appendix A – References



PC Chipset DMP Vortex86DX Processor	Vortex86DX Support Site
PC/104 Interface	PC/104 Specification
PC/104- <i>Plus</i> Interface	PC/104-<i>Plus</i> Specification

Appendix B – Custom Programming



GPIO Registers for PORT1 Interrupts

The PLD interrupt output connects to General Purpose Input/Output (GPIO) bit 6 on PORT1 on the Vortex86DX. This GPIO can be used to generate interrupts in the Vortex86DX. The GPIO is an input by default so no configuration for direction is necessary. However, it must be configured for use as an interrupt. See the DMP Vortex86 Series Software Programming Reference on the [DMP Vortex86DX CPU Support Page](#) for instructions on programming a GPIO for interrupts.

INTERRUPT MASK REGISTER

This register is used to mask interrupts generated by the PLD. This determines which interrupt status signals can generate a PLD interrupt.

IRQMASK (Read/Write) 1E3h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	IMASK_PERR	IMASK_SERR	IMASK_TC2	IMASK_TC1	IMASK_TCO

Table 29: Interrupt Mask Register Bit Assignments

Bit	Mnemonic	Description
D7-D5	Reserved	These bits are reserved and only 0 should be written to them.
D4	IMASK_PERR	Mask for the PCI Bus PERR interrupt. 0 = Disable interrupt 1 = Enable interrupt
D3	IMASK_SERR	Mask for the PCI Bus SERR interrupt. 0 = Disable interrupt 1 = Enable interrupt
D2	IMASK_TC2	Mask for the 8254 Timer #2 output (terminal count) interrupt. 0 = Disable interrupt 1 = Enable interrupt
D1	IMASK_TC1	Mask for the 8254 Timer #1 output (terminal count) interrupt. 0 = Disable interrupt 1 = Enable interrupt
D0	IMASK_TCO	Mask for the 8254 Timer #0 output (terminal count) interrupt. 0 = Disable interrupt 1 = Enable interrupt

INTERRUPT STATUS REGISTER

This register is used for reading the status of interrupts generated by the PLD.

IRQSTAT (Read-Status/Write-Clear) 1E4h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ISTAT_PERR	ISTAT_SERR	ISTAT_TC2	ISTAT_TC1	ISTAT_TCO

Table 30: Interrupt Status Register Bit Assignments

Bit	Mnemonic	Description
D7-D5	Reserved	These bits are reserved and only 0 should be written to them.
D4	ISTAT_PERR	Status for the PCI Bus PERR interrupt when read. 0 = PERR has not asserted 1 = PERR has asserted This bit is read-status; write 1 to clear.
D3	ISTAT_SERR	Status for the PCI Bus SERR interrupt when read. 0 = SERR has not asserted 1 = SERR has asserted This bit is read-status; write 1 to clear.
D2	ISTAT_TC2	Status for the 8254 Timer #2 output (terminal count) interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transitioned from a 0 to a 1 level This bit is read-status; write 1 to clear.
D1	ISTAT_TC1	Status for the 8254 Timer #1 output (terminal count) interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transitioned from a 0 to a 1 level This bit is read-status; write 1 to clear.
D0	ISTAT_TCO	Status for the 8254 Timer #0 output (terminal count) interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transitioned from a 0 to a 1 level This bit is read-status; write 1 to clear.

The interrupt status register is valid whether or not the interrupt mask is set in the IRQMSK register (that is, it can be used for polling status). An interrupt status is acknowledged (cleared to a 0) by writing a '1' to the status bit.

The Vortex86DX processor used on the VL-EPIC-17 does not support monitoring of the PERR and SERR error signals on the PCI bus. The PLD will monitor for any assertions on these signals.

The PLD implements an 8254 timer (consisting of three individual timers). The outputs of these timers can generate interrupts when they transition from low-to-high (edge sensitive).

8254 Timer Control Register

This register is used to set modes related to the inputs on the 8254 Timers.

TIMCNTRL (Read/Write) 1E5h

D7	D6	D5	D4	D3	D2	D1	D0
TIM2GATE	TIM1GATE	TIM0GATE	TM1MODE	TM1SEL	TM0SEL	Reserved	Reserved

Table 31: 8254 Timer Control Register Bit Assignments

Bit	Mnemonic	Description
D7	TIM2GATE	Sets the level on the Gate input for the 8254 Timer #2. 0 = Gate is disabled (set to a logic 0) 1 = Gate is enabled (set to a logic 1)
D6	TIM1GATE	Sets the level on the Gate input for the 8254 Timer #1. 0 = Gate is disabled (set to a logic 0) 1 = Gate is enabled (set to a logic 1)
D5	TIM0GATE	Sets the level on the Gate input for the 8254 Timer #0. 0 = Gate is disabled (set to a logic 0) 1 = Gate is enabled (set to a logic 1)
D4	TM1MODE	Configure how the 8254 Timer #1 and #2 are used. 0 – Timer #1 is cascaded with Timer #2 for a 32-bit timer 1 – Timer #1 operates in normal 16-bit mode
D3	TM1SEL	Configured the clock source for 8254 Timer #1. 0 – Timer #1 input clock is from User I/O connector input TMRIN1 1 – Timer #1 input clock is 4.16625 MHz internal clock (PCI clock divided by 8)
D2	TM0SEL	Configured the clock source for 8254 Timer #0. 0 – Timer #0 input clock is from User I/O connector input TMRIN0 1 – Timer #0 input clock is 4.16625 MHz internal clock (PCI clock divided by 8)
D1-D0	Reserved	These bits are reserved and only 0 should be written to them.

An 8254 timer is implemented in the PLD. It contains three independent 16-bit timers. It is fully software compatible with the Intel 8254, except that only binary counting modes are implemented (the BCD control bit is implemented but ignored). See the [Intel 82C54 Programmable Interval Timer Datasheet](#) for register definitions and programming information.

There is an option to cascade two of the timers together in a 32-bit mode. The timers are identified as Timer 0, 1, and 2. When Timers 1 and 2 are cascaded, Timer 1 is the LS 16-bits and Timer 2 is the MS 16-bits. In this 32-bit cascade mode the timer output of Timer 1 feeds the clock input of Timer 2. In this mode, Timer 1 would normally be set so that it generates a clock after counting the full 16-bit range, but there is no requirement to do this.

The 32-bit cascade mode is set in TM1MODE in the Timer Control Register. There are also internal or external clock selections for the timers in this register using the external clocks TMRIN0 and TMRIN1 signals on the user I/O connector at J7. The internal clock is the PCI clock divided by 8 ($33.33 \text{ MHz} / 8 = 4.16625 \text{ MHz}$). TMRIN0 can only be used with Timer 0. TMRIN1 can only be used with Timer 1. The clock for Timer 2 is always the internal clock except in the 32-bit cascade mode when the output from Timer 1 is the clock for Timer 2.

The timer outputs can generate interrupts. When a timer output transitions from a 0 to a 1 then an interrupt status bit is set which can generate an interrupt. This bit sticks until cleared.

8254 Timer Base Address

This register is used to set the I/O base address on the 8254 Timers. The timers only require 4 continuous bytes of I/O memory space (byte addressing only). The address must be 4-byte aligned. Two 8-bit registers must be set. The Vortex86DX BIOS is configured to map the I/O range of 1D0-1DF to the PLD. The addresses 1DC-1DF in this I/O space are dedicated to the four 8254 Timer byte addresses and the timer base address is set to 1DC by default. The timer base address can be changed to another area in the I/O space if desired should the 1DC-1DF range be required for other purposes.

TIMBASEMS (Read/Write) 1E6h

D7	D6	D5	D4	D3	D2	D1	D0
TIMBASE15	TIMBASE14	TIMBASE13	TIMBASE12	TIMBASE11	TIMBASE10	TIMBASE9	TIMBASE8

Table 32: 8254 Timer Base MS Address Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	TIMBASE(15:8)	Most significant 8 bits of the 16-bit Timer Base Address. Default is 01h (default timer base address is 1DCh)

TIMBASELS (Read/Write) 1E7h

D7	D6	D5	D4	D3	D2	D1	D0
TIMBASE7	TIMBASE6	TIMBASE5	TIMBASE4	TIMBASE3	TIMBASE2	TIMBASE1	TIMBASE0

Table 33: 8254 Timer Base LS Address Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	TIMBASE(7:0)	Least significant 8 bits of the 16-bit Timer Base Address. Default is DCh (default timer base address is 1DCh). The LS 2-bits TIMBASE(1:0) must always be set to zero; any other value will be ignored.