Reference Manual

VL-7914
VL-79CT14

Decoded Prototyping
Card for the STD Bus

STD

VERSALOGIC
CORPORATION

VL-7914
VL-79CT14

Decoded Prototyping Card
for the STD Bus

Model VL-7914

Decoded Protyping Card for the STD Bus

REFERENCE MANUAL

VL-0000 Rev. 0.00
VL-79CT14 Rev. 0.00
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M7914

Table of Contents

Overview

Introduction

This manual details the installation and operation of VersaLogic's VL-7914 interface card. The VL-7914 decoded I/O utility card is designed for construction of experimental and custom I/O interfaces with a minimum of effort. It combines a large prototyping area with on-board STD Bus buffering and decoding circuitry to greatly simplify prototype design and construction.

This card is available in standard (VL-7914) and extended temperature (VL-79CT14) versions. Throughout this manual "VL-7914" will be used to refer to both versions of these boards, unless specifically noted otherwise.

Overview

The VL-7914 board provides 16 completely decoded strobe lines (8 read lines and 8 write lines) for connection to user constructed circuitry. They allow I/O circuitry to be built with no additional bus interface required. The on-board circuitry also controls the data buffers to gate data to and from the bus at the appropriate time.

A large grid area is available for construction of the user circuitry. Power and ground pads, along with clearly labeled signal pads, make the VL-7914 an extremely effective way to build custom interfaces for the STD Bus.

Features

- Eight decoded input strobes.
- Eight decoded output strobes.
- 8, 10, and 16-bit I/O addressing.
- 16-bit memory addressing.
- IOEXP and MEMEX line supported.
- Clearly marked connection points.
- Large prototyping area.
- Accommodates standard wire wrap posts.
- Extended temperature range version available.
- Universal STD Bus processor compatible.
- Enhanced plug-in replacement for Pro-Log 7914.

Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Size: Meets all STD Bus mechanical specifications
Storage Temperature:
VL-7914: -40° to +75°C
VL-79CT14: -40° to +85°C
Free Air Operating Temperature:
VL-7914: 0° to +65°C
VL-79CT14: -40° to +85°C
Power Requirements:
VL-7914: 5V +-5% @ 110 ma typ. (plus user circuitry)
VL-79CT14: 5V +-10% @ 5 ma typ. (plus user circuitry)
Addressing: 8, 10, or 16-bit I/O or memory addressing
Mapping: Occupies 8 addresses on any modulo 8 boundary
Decoding: 8 read and 8 write strobes provided

Installation and Configuration

Handling

** **CAUTION** ** The VL-7914 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

Installation

The VL-7914 card can be installed in any slot of an STD Bus card cage.

The VL-7914 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

** **CAUTION** ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** **CAUTION** ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

External Connections

Connection to the VL-7914 can be made to user installed connectors on the board. For easiest use, header type connector(s) should be installed on the card ejector end of the board.

Jumper Summary

Various options available on the VL-7914 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 2-2 shows the jumper block locations on the VL-7914 board. It indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 2-1.

Jumper Block	Description	As Shipped	Page
V1	Data buffer control.		2-9
V2	MEMEX select.		2-9
	a - High or low.	a - IN	
	b - Active low.	b - out	
	- - Active high (both jumpers out).		
V3	16-bit address select.		2-4
V4	16-bit address mode select.		2-4
	a - Memory mapped.	a - IN	
	b - I/O mapped.	b - out	
V5	IOEXP select.		2-7
	a - High or low.	a - IN	
	b - Active low.	b - out	
	- - Active high (both jumpers out).		
V6	A8-A9 address select.		2-4
	a - A9 control.	a - ignore A9	
	b - A8 control.	b - ignore A8	
V7	A3-A7 address select.		2-4
V8	I/O address mode select.		
	a - 8 or 10-bit I/O address.	a - IN	
	b - 16-bit memory or I/O address.	b - out	

Figure 2-1. Jumper Functions

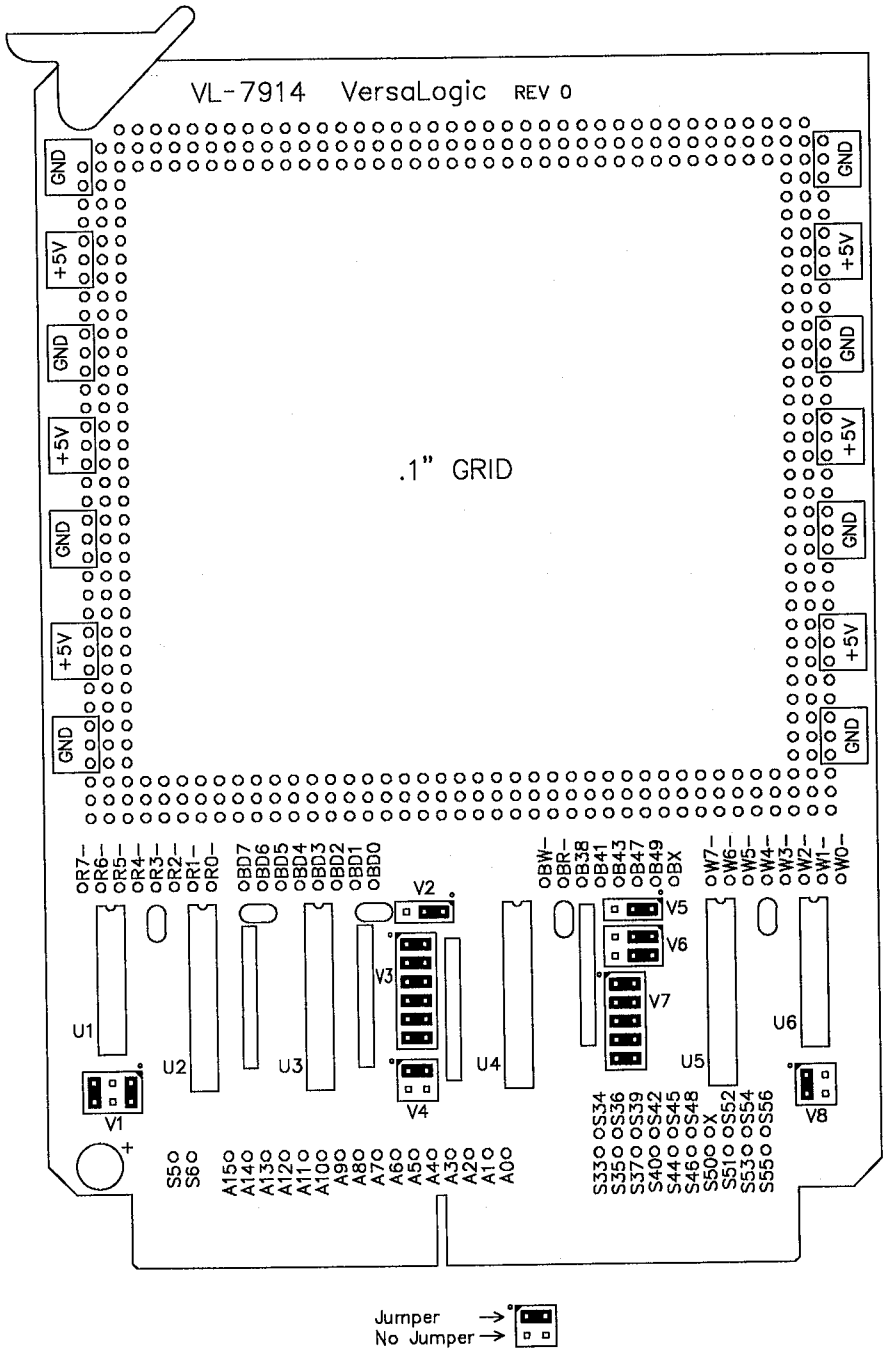


Figure 2-2. Jumper Block Locations

Board Addressing

The VL-7914 supports 8-, 10-, and 16-bit I/O addressing, and 16-bit memory addressing. 8-bit I/O addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10- or 16-bit addressing can be used with 16-bit processors (8088, 80188, 80186, etc.) to decode 1024 or 65536 I/O port addresses. 16-bit memory addressing can be used with most 8-bit processors (Z80, 8085, 6809, etc.) if desired.

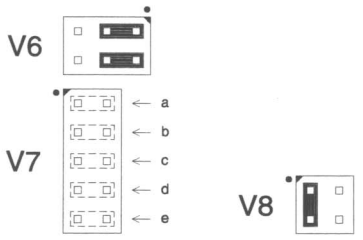
I/O addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7914. Memory addressing can be extended (capacity doubled) using the MEMEX signal which is decoded by the VL-7914.

As shipped the board is configured for 8-bit I/O addressing with a board address of hex 00. The card occupies eight consecutive addresses (i.e. 00H to 07H).

8-Bit I/O Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired address (i.e. "3" and "0" = hex address 30). Jumpers V6 and V8 should be set as shown. Refer to the IOEXP Signal section on page 2-7 to set the IOEXP jumper.

Jumpers V2, V3 and V4 are not used in this mode and can remain jumpered in any configuration.



V7 a	V7 b	V7 c	V7 d	Upper Digit	V7 e	Lower Digit
X	X	X	X	0	X	0
X	X	X	-	1	-	8
X	X	-	X	2		
X	X	-	-	3		
X	-	X	X	4		
X	-	X	-	5		
X	-	-	X	6		
X	-	-	-	7		
-	X	X	X	8		
-	X	X	-	9		
-	X	-	X	A		
-	X	-	-	B		
-	-	X	X	C		
-	-	X	-	D		
-	-	-	X	E		
-	-	-	-	F		

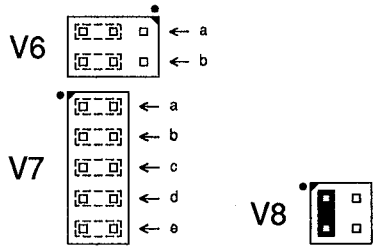
X = Jumper installed
- = Jumper removed

Figure 2-3. 8-Bit I/O Address Jumpers

10-Bit I/O Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" and "3" and "0" = hex address 130). Jumper V8 should be set as shown. Refer to the IOEXP Signal section on page 2-7 to set the IOEXP jumper.

Jumpers V2, V3 and V4 are not used in this mode and can remain jumpered in any configuration.



V6 a	V6 b	Upper Digit
X	X	0
X	-	1
-	X	2
-	-	3

V7 a	V7 b	V7 c	V7 d	Middle Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

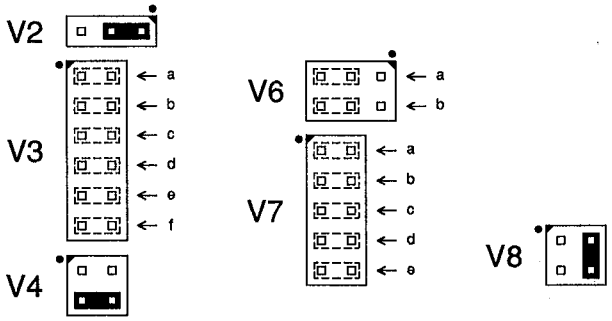
V7 e	Lower Digit
X	0
-	8

X = Jumper installed
- = Jumper removed

Figure 2-4. 10-Bit I/O Address Jumpers

16-Bit I/O Addressing

To configure the board for a 16-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired address (i.e. "6" and "1" and "3" and "0" = hex address 6130). Jumpers V2, V4 and V8 should be set as shown. Refer to the IOEXP Signal section on page 2-7 to set the IOEXP jumper.



V3 a	V3 b	V3 c	V3 d	Top Digit	V3 e	V3 f	V6 a	V6 b	Second Digit	V7 a	V7 b	V7 c	V7 d	Third Digit	V7 e	Bottom Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	-	1	X	X	X	-	1	X	X	X	-	1	-	8
X	X	-	X	2	X	X	-	X	2	X	X	-	X	2		
X	X	-	-	3	X	X	-	-	3	X	X	-	-	3		
X	-	X	X	4	X	-	X	X	4	X	-	X	X	4		
X	-	X	-	5	X	-	X	-	5	X	-	X	-	5		
X	-	-	X	6	X	-	-	X	6	X	-	-	X	6		
X	-	-	-	7	X	-	-	-	7	X	-	-	-	7		
-	X	X	X	8	-	X	X	X	8	-	X	X	X	8		
-	X	X	-	9	-	X	X	-	9	-	X	X	-	9		
-	X	-	X	A	-	X	-	X	A	-	X	-	X	A		
-	X	-	-	B	-	X	-	-	B	-	X	-	-	B		
-	-	X	X	C	-	-	X	X	C	-	-	X	X	C		
-	-	X	-	D	-	-	X	-	D	-	-	X	-	D		
-	-	-	X	E	-	-	-	X	E	-	-	-	X	E		
-	-	-	-	F	-	-	-	-	F	-	-	-	-	F		

X = Jumper installed
- = Jumper removed

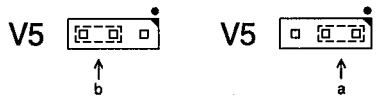
Figure 2-5. 16-Bit I/O Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown below.

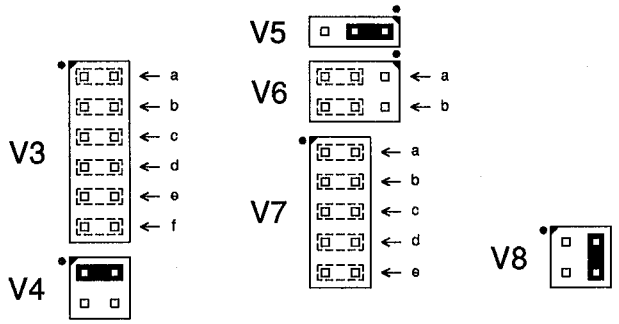


Jumper Block	Description	As Shipped
V5	IOEXP select	
	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 2-6. IOEXP Options

16-Bit Memory Addressing

To configure the board for a 16-bit memory address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired address (i.e. "6" and "1" and "3" and "0" = hex address 6130). Jumpers V4, V5 and V8 should be set as shown. Refer to the MEMEX Signal section on page 2-9 to set the MEMEX jumper.



V3 a	V3 b	V3 c	V3 d	Top Digit	V3 e	V3 f	V6 a	V6 b	Second Digit	V7 a	V7 b	V7 c	V7 d	Third Digit	V7 e	Bottom Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	-	1	X	X	X	-	1	X	X	X	-	1	-	8
X	X	-	X	2	X	X	-	X	2	X	X	-	X	2		
X	X	-	-	3	X	X	-	-	3	X	X	-	-	3		
X	-	X	X	4	X	-	X	X	4	X	-	X	X	4		
X	-	X	-	5	X	-	X	-	5	X	-	X	-	5		
X	-	-	X	6	X	-	-	X	6	X	-	-	X	6		
X	-	-	-	7	X	-	-	-	7	X	-	-	-	7		
-	X	X	X	8	-	X	X	X	8	-	X	X	X	8		
-	X	X	-	9	-	X	X	-	9	-	X	X	-	9		
-	X	-	X	A	-	X	-	X	A	-	X	-	X	A		
-	X	-	-	B	-	X	-	-	B	-	X	-	-	B		
-	-	X	X	C	-	-	X	X	C	-	-	X	X	C		
-	-	X	-	D	-	-	X	-	D	-	-	X	-	D		
-	-	-	X	E	-	-	-	X	E	-	-	-	X	E		
-	-	-	-	F	-	-	-	-	F	-	-	-	-	F		

X = Jumper installed
- = Jumper removed

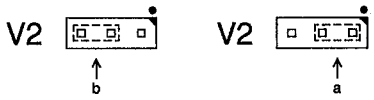
Figure 2-7. 16-Bit Memory Address Jumpers

MEMEX Signal

The MEMEX (memory expansion) signal on the STD Bus is normally used to select between two different memory banks or maps. It can be used to double the number of available memory addresses in the system (by selecting between the two memory banks). The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low MEMEX signal usually selects the standard or normal memory map. A high MEMEX signal usually selects the secondary or alternate memory map. Boards that ignore (or do not decode) MEMEX will appear in both memory maps.

As shipped the MEMEX jumper is configured to ignore the MEMEX signal. The board will be addressed whether the MEMEX signal is high or low. It can be jumpered for two other modes as shown below.



Jumper Block	Description	As Shipped
V2	MEMEX select	
	a - Ignore MEMEX (enable high or low).	a - IN
	b - Enable on MEMEX low.	b - out
	None - Enable on MEMEX high (no jumpers).	

Figure 2-8. MEMEX Options

Data Buffer Control

Jumper block V1 allows the selection (enabling) and direction of buffer chip (U2) to be controlled. As shipped this jumper is positioned to enable the buffer whenever the card is selected (board address through board address +8). The direction of the buffer (buffering from or to the STD Bus) is controlled by the RD* (read) signal from the bus.

For special applications refer to the VL-7914 schematic. U2 pin 1 controls the buffer direction. U2 pin 19 enables or tri-states the outputs.

For normal applications, where the on-board read and write strobes are used, V1 should be jumpered as shown in Figure 2-2.

Operation

Physical Construction

The VL-7914 will accept standard solder type or .025" square post wire wrap type sockets, and single press-fit wire wrap pins. Access to the on-board signals can be by direct solder connection, or by wire wrapping to single press-fit wire wrap pins which can be installed in the desired signal access holes. The wire wrap pins or sockets may be soldered into the holes if desired.

Both the 3.7" x 3.8" user grid area, and the signal access points are constructed of .042" holes.

The .1" grid will also accommodate popular header type connectors. Normally the card ejector edge of the board is used for straight or right angle headers. One 50-pin connector or several smaller connectors can be accommodated at the board edge.

Decoupling capacitors should be included within the user constructed circuit area to control switching noise on the power supply lines.

All of the bus interface chips on the VL-7914 are socketed and may be removed or replaced as desired. Unused chips (such as U3 with I/O addressing) may be removed to save power. The chips may also be removed for safety during initial power-up and testing.

Board Mapping

The VL-7914 occupies eight address locations. The eight locations are used for the eight read and eight write strobe lines that are available for connection to the user constructed circuitry. These are normally eight I/O port address, although the board can alternately be jumpered for memory mapped addressing.

The locations of the eight addresses are determined by the board address, which is jumper selectable. As shipped, the board is jumpered for an 8-bit I/O address of hex 00. In this configuration the board would occupy I/O ports 00 through 07.

Once the board's address has been determined, the addresses of the eight strobes can be determined as shown in Figure 3-1. Each address can be both read (for inputting data) and written (for outputting data).

Address	Read Strobe	Write Strobe
Board Address +0	R0-	W0-
Board Address +1	R1-	W1-
Board Address +2	R2-	W2-
Board Address +3	R3-	W3-
Board Address +4	R4-	W4-
Board Address +5	R5-	W5-
Board Address +6	R6-	W6-
Board Address +7	R7-	W7-

Figure 3-1. Strobe Address Locations

Access Points

The user constructed circuitry is interfaced to the bus via the on-board buffering and decoding circuitry. These signals are arranged in several groups of access points that may be connected to the user circuitry as needed.

For typical I/O circuits only the read and/or write strobe signals, the data lines (BD0-BD7), and the system reset signal will be required. For special applications other signals may be required. Refer to the VL-7914 schematic or the Access Point List in the Reference section starting on page 4-1 for the specific signals available.

Note that access points "X" and "BX" make an uncommitted buffer available to the user. Point "X" is the input to the buffer, point "BX" is the output from the buffer.

I/O Strobes

The decoded strobe lines for reading and writing data can be connected directly to the user's circuitry. They are designed to interface standard I/O chips to the bus.

The write strobes (W0- through W7-) allow data to be written into user connected I/O chips. These active low signals will go low when the CPU writes data to the address corresponding to the particular write strobe line (board address +0 through board address +7). Data, from the on-board data buffers, should be latched (by the user's circuitry) at the end (rising edge) of this strobe.

The read strobes (R0- through R7-) allow data to be read from user connected I/O chips. These active low signals will go low when the CPU reads data from the address corresponding to the particular read strobe line (board address +0 through board address +7). Data, connected to the on-board data buffers, should be made available when the strobe line is in its low state. If there is more than one on-board I/O chip connected to the data buffers, then all on-board I/O chips should disable their output drivers (tri-state their outputs) when their read strobe is high.

Reference

Access Point List

Access Point	Description
A0 to A15	Address lines from the STD Bus (unbuffered)
BD0 to DB7	Buffered data lines (bidirectional)
R0– to R7–	Decoded read strobe lines (active low)
W0– to W7–	Decoded write strobe lines (active low)

Access Point	Description	
S33	STD Bus pin 33, IORQ*	(I/O address select)
S34	STD Bus pin 34, MEMRQ*	(Memory addr. select)
S35	STD Bus pin 35, IOEXP*	(I/O expansion)
S36	STD Bus pin 36, MEMEX*	(Memory expansion)
S37	STD Bus pin 37, REFRESH*	(Refresh timing)
S39	STD Bus pin 39, STATUS1*	(CPU status)
S40	STD Bus pin 40, STATUS0*	(CPU status)
S42	STD Bus pin 42, BUSRQ*	(Bus request)
S44	STD Bus pin 44, INTRQ*	(Interrupt request)
S45	STD Bus pin 45, WAITRQ*	(Wait request)
S46	STD Bus pin 46, NMIRQ*	(Non-maskable interrupt)
S48	STD Bus pin 48, PBRESET*	(Push button reset)
S50	STD Bus pin 50, CNTRL*	(AUX timing)
X	Input to buffer X	(See BX access point)
S51	STD Bus pin 51, PCO	(Priority chain out)
S52	STD Bus pin 52, PCI	(Priority chain in)
S53	STD Bus pin 53, AUXGND	(±12 volt ground)
S54	STD Bus pin 54, AUXGND	(±12 volt ground)
S55	STD Bus pin 55, AUX+V	(+12 volt input)
S56	STD Bus pin 56, AUX–V	(–12 volt input)
BW–	Buffered STD Bus pin 31, WR*	(Write strobe)
BR–	Buffered STD Bus pin 32, RD*	(Read strobe)
B38	Buffered STD Bus pin 38, MCSYNC*	(Machine cycle sync)
B41	Buffered STD Bus pin 41, BUSAK*	(Bus acknowledge)
B43	Buffered STD Bus pin 43, INTAK*	(Interrupt acknowledge)
B47	Buffered STD Bus pin 47, SYSRESET*	(System reset)
B49	Buffered STD Bus pin 49, CLOCK*	(CPU clock)
BX	Buffered signal from access point "X"	
S5	STD Bus pin 5, VBAT	(Battery backup)
S6	STD Bus pin 6, DCPD*	(DC power down)

Note: * = active low signal.

Figure 4-1. Access Points.

STD 80 Bus Pinout

Connections from the VL-7914 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7914.

COMPONENT SIDE				SOLDER SIDE			
Pin	**Signal**	**Flow**	**Description**	**Pin**	**Signal**	**Flow**	**Description**
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBAT	I/O	Battery backup	6	DCPD*	I/O	DC power down
7	D3/A19	I/O	Data bus	8	D7	I/O	Data bus
9	D2/A18	I/O	Data bus	10	D6	I/O	Data bus
11	D1/A17	I/O	Data bus	12	D5/A21	I/O	Data bus
13	D0/A16	I/O	Data bus	14	D4/A20	I/O	Data bus
15	A7	In	Address bus	16	A15	In	Address bus
17	A6	In	Address bus	18	A14	In	Address bus
19	A5	In	Address bus	20	A13	In	Address bus
21	A4	In	Address bus	22	A12	In	Address bus
23	A3	In	Address bus	24	A11	In	Address bus
25	A2	In	Address bus	26	A10	In	Address bus
27	A1	In	Address bus	28	A9	In	Address bus
29	A0	In	Address bus	30	A8	In	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	In	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	In	Memory expansion
37	REFRESH*	In	Refresh timing	38	MCSYNC*	In	Machine cycle sync.
39	STATUS1*	In	CPU status	40	STATUS0*	In	CPU status
41	BUSAK*	In	Bus acknowledge	42	BUSRQ*	Out	Bus request
43	INTAK*	In	Interrupt acknowl.	44	INTRQ*	Out	Interrupt request
45	WAITRQ*	Out	Wait request	46	NMIRQ*	Out	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	I/O	Push button reset
49	CLOCK*	In	CPU clock	50	CNTRL*	I/O	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	I/O	±12 volt ground	54	AUXGND	I/O	±12 volt ground
55	AUX+V	I/O	+12 volt input	56	AUX–V	I/O	–12 volt input

Notes:
* Denotes an active low signal.

Figure 4-2. STD 80 Bus Pinout.

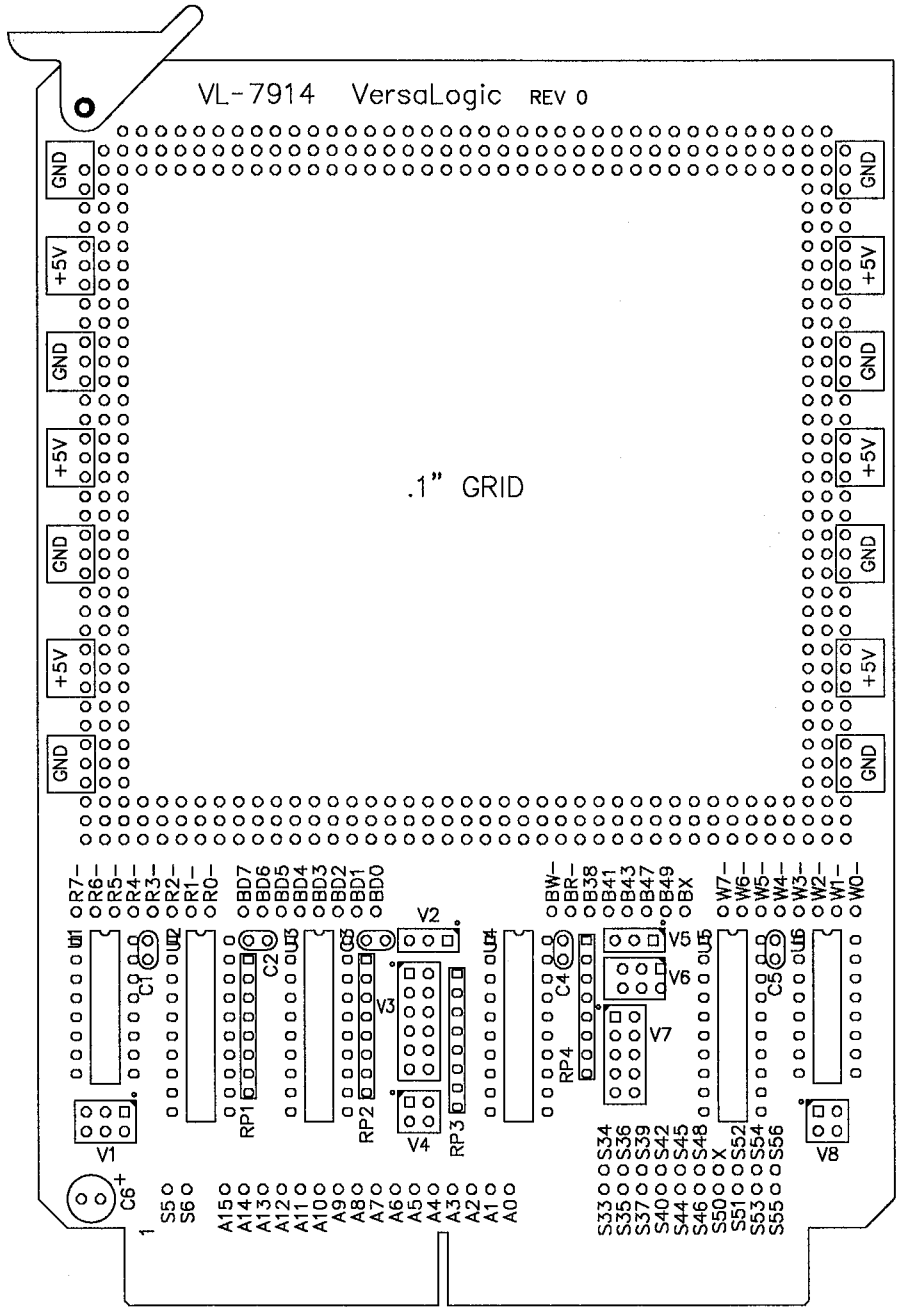
Decimal / Hex / ASCII Conversion Chart

The chart below is useful for both ASCII and decimal / hex conversion. The "^" symbol denotes control characters. "^A" represents control-A, etc.

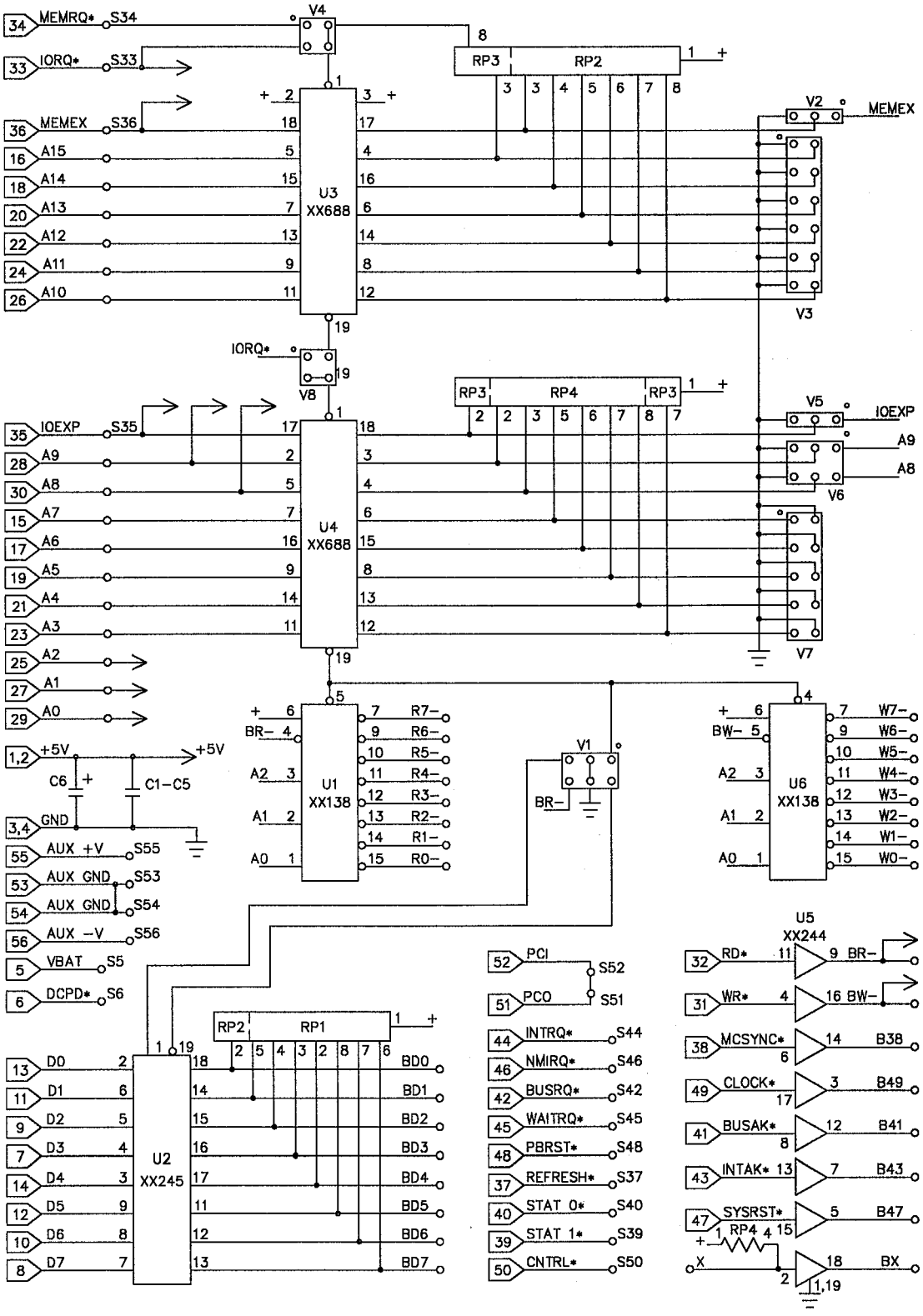
Dec.	Hex	ASCII		Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL		32	20	SPACE	64	40	@	96	60	`
1	01	SOH	^A	33	21	!	65	41	A	97	61	a
2	02	STX	^B	34	22	"	66	42	B	98	62	b
3	03	ETX	^C	35	23	#	67	43	C	99	63	c
4	04	EOT	^D	36	24	$	68	44	D	100	64	d
5	05	ENQ	^E	37	25	%	69	45	E	101	65	e
6	06	ACK	^F	38	26	&	70	46	F	102	66	f
7	07	BEL	^G	39	27	'	71	47	G	103	67	g
8	08	BS	^H	40	28	(	72	48	H	104	68	h
9	09	HT	^I	41	29	)	73	49	I	105	69	i
10	0A	LF	^J	42	2A	*	74	4A	J	106	6A	j
11	0B	VT	^K	43	2B	+	75	4B	K	107	6B	k
12	0C	FF	^L	44	2C	,	76	4C	L	108	6C	l
13	0D	CR	^M	45	2D	–	77	4D	M	109	6D	m
14	0E	SO	^N	46	2E	.	78	4E	N	110	6E	n
15	0F	SI	^O	47	2F	/	79	4F	O	111	6F	o
16	10	DLE	^P	48	30	0	80	50	P	112	70	p
17	11	DC1	^Q	49	31	1	81	51	Q	113	71	q
18	12	DC2	^R	50	32	2	82	52	R	114	72	r
19	13	DC3	^S	51	33	3	83	53	S	115	73	s
20	14	DC4	^T	52	34	4	84	54	T	116	74	t
21	15	NAK	^U	53	35	5	85	55	U	117	75	u
22	16	SYN	^V	54	36	6	86	56	V	118	76	v
23	17	ETB	^W	55	37	7	87	57	W	119	77	w
24	18	CAN	^X	56	38	8	88	58	X	120	78	x
25	19	EM	^Y	57	39	9	89	59	Y	121	79	y
26	1A	SUB	^Z	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC		59	3B	;	91	5B	[	123	7B	{
28	1C	FS		60	3C	<<	92	5C	\	124	7C	|
29	1D	GS		61	3D	=	93	5D	]	125	7D	}
30	1E	RS		62	3E	>>	94	5E	^	126	7E	~
31	1F	US		63	3F	?	95	5F	_	127	7F	DEL

Figure 4-3. Decimal / hex / ASCII Conversion Chart

VL-7914 Parts Placement Diagram



VL-7914 Schematic



VL-7914 Parts List

Capacitors

C1-C5	C-103	.01 µf Z5U
C6	CE220FR	22 µf electrolytic, radial

Integrated Circuits

U1,U6	ILS138	74LS138
U2	ILS245	74LS245
U3,U4	IHCT688	74HCT688
U5	ILS244	74LS244

Resistors

RP1-RP4	RN472-7	4.7K, 8 pin, 7 resistor SIP

Miscellaneous

V1,V6	XAA02M	2 x 3 pin straight header
V2,V5	XAA03MS	1 x 3 pin straight header
V3	XAA02M	2 x 6 pin straight header
V4,V8	XAA02M	2 x 2 pin straight header
V7	XAA02M	2 x 5 pin straight header
U1,U6	XD-16	16 pin DIP socket
U2-U5	XD-20	20 pin DIP socket

VL-79CT14 Parts List

Capacitors

C1-C5	C-103	.01 µf Z5U
C6	CE220FR	22 µf electrolytic, radial

Integrated Circuits

U1,U6	IHCT138	74HCT138
U2	IACT245	74ACT245 (74AHCT245)
U3,U4	IHCT688	74HCT688
U5	IACT244	74ACT244 (74AHCT244)

Resistors

RP1-RP4	RN104-7	100K, 8 pin, 7 resistor SIP

Miscellaneous

V1,V6	XAA02M	2 x 3 pin straight header
V2,V5	XAA03MS	1 x 3 pin straight header
V3	XAA02M	2 x 6 pin straight header
V4,V8	XAA02M	2 x 2 pin straight header
V7	XAA02M	2 x 5 pin straight header
U1,U6	XD-16	16 pin DIP socket
U2-U5	XD-20	20 pin DIP socket