Reference Manual

VL-7614

64-Line TTL Interface Card
for the STD Bus

VERSALOGIC
CORPORATION

VL-7614
VL-76CT14

64-Line TTL Interface Card
for the STD Bus

Model VL-7614

64-Line TTL Interface Card for the STD Bus

REFERENCE MANUAL

VL-7614 Rev. 2.00
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M7614

Model VL-7614
64-Line TTL Interface Card

REFERENCE MANUAL

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Section 1
OVERVIEW

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7614 interface card. This card provides 64 TTL type I/O lines for general purpose interfacing requirements.

The VL-7614 is available in standard (VL-7614) and extended temperature (VL-76CT14) versions. Throughout this manual "VL-7614" will be used to refer to both versions of these boards, unless specifically noted otherwise.

OVERVIEW

The VL-7614 card provides 64 TTL type input/output lines. Grouped as 8 ports of 8 lines, each port can be configured as 8 inputs, 8 outputs, or 8 outputs with readback.

I/O configuration is accomplished by physically removing or inserting selected chips from the board (one input and output chip per 8-bit port). This allows the board to be configured in any combination of input and output ports desired.

Each 8-bit port of non-inverting input lines can be read at any time by the system processor. Pull-up resistors are included to assure that unconnected lines do not have an undetermined state. Input ports can also be used in conjunction with output ports to "read back" the output data. LS244 type chips with .4V hysteresis (ACT244 in the extended temperature version) are used for the data input buffers.

The output lines are non-inverting and can drive 17 LS TTL loads (6.8 ma sink, 3.5 ma CT version). When a port is used for output, it can optionally be configured with the corresponding input buffer left in place. This allows the state of the output lines for that port to be read by the processor. This function, usually called port readback, can be used to simplify programming and assure correct program operation in many applications. LS273 type chips (HCT273 in the extended temperature version) are used for the data output latches.

External connections are made through four 34-pin latching connectors. Each connector interfaces sixteen I/O lines (two 8-bit ports) to external devices. Alternating ground lines, paired with each signal line, improve noise immunity and reduce cross talk.

The VL-7614 features 8 and 10-bit addressing, and is compatible with all common STD Bus processor types. The IOEXP line is also supported.

The VL-7614 normally occupies eight consecutive I/O addresses. It can alternately be mapped into only four I/O addresses when it is configured as four input ports and four output ports.

The board is fully compatible with the Pro-Log 7614 card.

FEATURES

- Eight 8-bit I/O Ports.
- 6.8 ma output drive (3.5 ma CT version).
- 8 or 10-bit I/O addressing.
- IOEXP supported.
- Latching I/O connectors.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Plug-in replacement for Pro-Log 7614.

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature:
- VL-7614: -40· to +75· C
- VL-76CT14: -40· to +85· C

Free Air Operating Temperature:
- VL-7614: 0· to +65· C
- VL-76CT14: -40· to +85· C

Power Requirements:
- VL-7614: 5V ±5% @ 450 ma typ. (all outputs high)
  5V ±5% @ 540 ma typ. (all outputs low)

- VL-76CT14: 5V ±10% @ 5.5 ma typ. (all outputs high)
  5V ±10% @ 38.5 ma typ. (all outputs low)

I/O Port Interface:
- VL-7614: Low level output drive: 6.8 ma @ .35V
  High level output drive: .9 ma @ 2.7V
  Input load: 1.2 ma @ .35V (4.7K ohm pull-up)

- VL-76CT14: Low level output drive: 3.5 ma @ .1V
  High level output drive: 4.0 ma @ 4.9V
  Input load .5 ma @ .1V (10K ohm pull-up)

Section 2
CONFIGURATION

JUMPER SUMMARY

Various options available on the VL-7614 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

The function of each jumper block is detailed in Figure 2-1. Figure 2-2 shows the jumper block locations on the VL-7614 board. It indicates the position of the jumper plugs as shipped from the factory.

Jumper Block	Description	As Shipped
V1	10-bit address control. See Board Address. a - A9 control. b - A8 control.	 a - ignore A9 b - ignore A8
V2	Board address. See Board Address.	Hex 00
V3	Addressing control. See Board Address. a - A2 control (4-port mode only). b - IOEXP control.	 Ignore A2 Ignore IOEXP
V4	4 or 8-port mapping. See Mapping Mode.	8-port mode

Figure 2-1. Jumper Functions

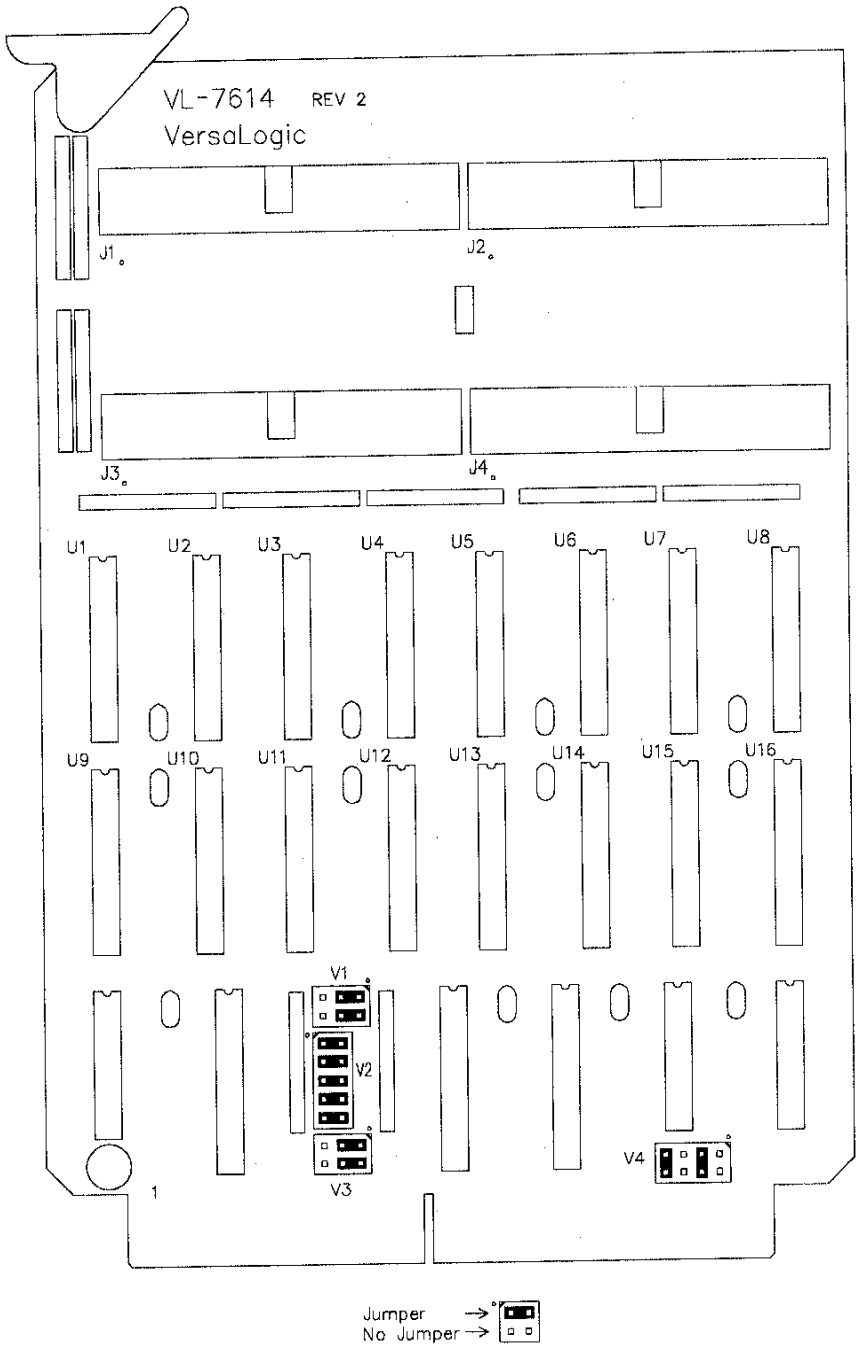


Figure 2-2. Jumper Block Locations

BOARD ADDRESS

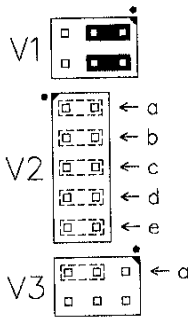
The VL-7614 supports both 8 and 10-bit I/O addressing. 8-bit addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10-bit addressing can be used with 16-bit processors (i.e. 8088) to decode up to 1024 I/O port addresses.

Both 8 and 10-bit addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7614.

As shipped the board is configured for 8-bit addressing with a board address of hex 00. The VL-7614 normally occupies eight consecutive I/O addresses (i.e. 00-07). If it is configured as four input ports and four output ports it can optionally be mapped into only four I/O ports.

8-Bit Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e. "3" and "0" = hex address 30).



V2				Upper
a	b	c	d	Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

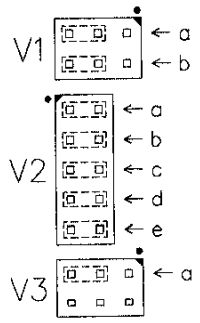
V2	V3	Lower
e	a*	Digit
X	X	0
X	-	4
-	X	8
-	-	C

X = Jumper installed.
- = Jumper removed.
* Jumper V3a is used only with optional 4-port mapping. Otherwise the lower hex digit will be 0 or 8 (per the position of V2e).

Figure 2-3. 8-Bit Address Jumpers

10-Bit Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" and "3" and "0" = hex address 130).



V1 a	V1 b	Upper Digit
X	X	0
X	-	1
-	X	2
-	-	3

V2 a	V2 b	V2 c	V2 d	Middle Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

V2 e	V3 a*	Lower Digit
X	X	0
X	-	4
-	X	8
-	-	C

X = Jumper installed.
- = Jumper removed.
* Jumper V3a is used only with optional 4-port mapping. Otherwise the lower hex digit will be 0 or 8 (per the position of V2e).

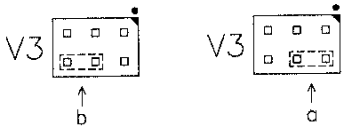
Figure 2-4. 10-Bit Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 2-5.



Jumper Block	Description	As Shipped
V3	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 2-5. IOEXP Options

MAPPING MODE

The VL-7614 normally occupies eight I/O port addresses. In this mode the I/O ports can be configured in any way desired (all inputs, all outputs or any mix).

Optionally the board can be configured to occupy only four I/O port addresses. In this mode the I/O ports must be configured as four input channels and four output channels. This mode is advantageous only when there are many I/O boards in the system and the I/O map is becoming full.

Unless system I/O addresses are very scarce (all 256 or more being used), the board should be used in the 8-port mode.

8-Port Mapping

To configure the board for 8-port mapping, jumper the board as shown below. In this mode jumper V3a is ignored when selecting the starting address for the board and should be located as shown below.

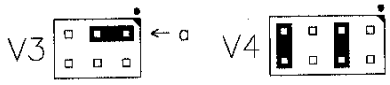


Figure 2-6. 8-Port Mapping

4-Port Mapping

To configure the board for 4-port mapping, jumper the board as shown below. In this mode jumper V3a is used for addressing the board and should be inserted or removed from the position shown according to the addressing tables in the preceding sections.

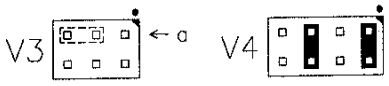


Figure 2-7. 4-Port Mapping

I/O PORTS

The I/O ports are configured for input or output by removing selected chips from the board. The board is arranged as 8 channels of 8 lines each (64 lines total). Each group of 8 lines can be configured as either input or output lines.

As shipped, with all the chips on the board, the VL-7614 is configured as 8 output channels. To configure any of the channels for input the output chip (for that channel) is removed from the board.

Normally it is desirable to leave the input chip installed on channels used for output. This allows the current state of the output lines to be read if desired. If this feature is not needed, the input chips can be removed to save a small amount of power.

In the standard 8-port mode, any of the eight channels (0-7) can be configured as inputs or outputs as desired. The figure below shows an example of a typical configuration. It shows the location of the input and output chips for each channel, and how the channels would appear on the I/O connectors.

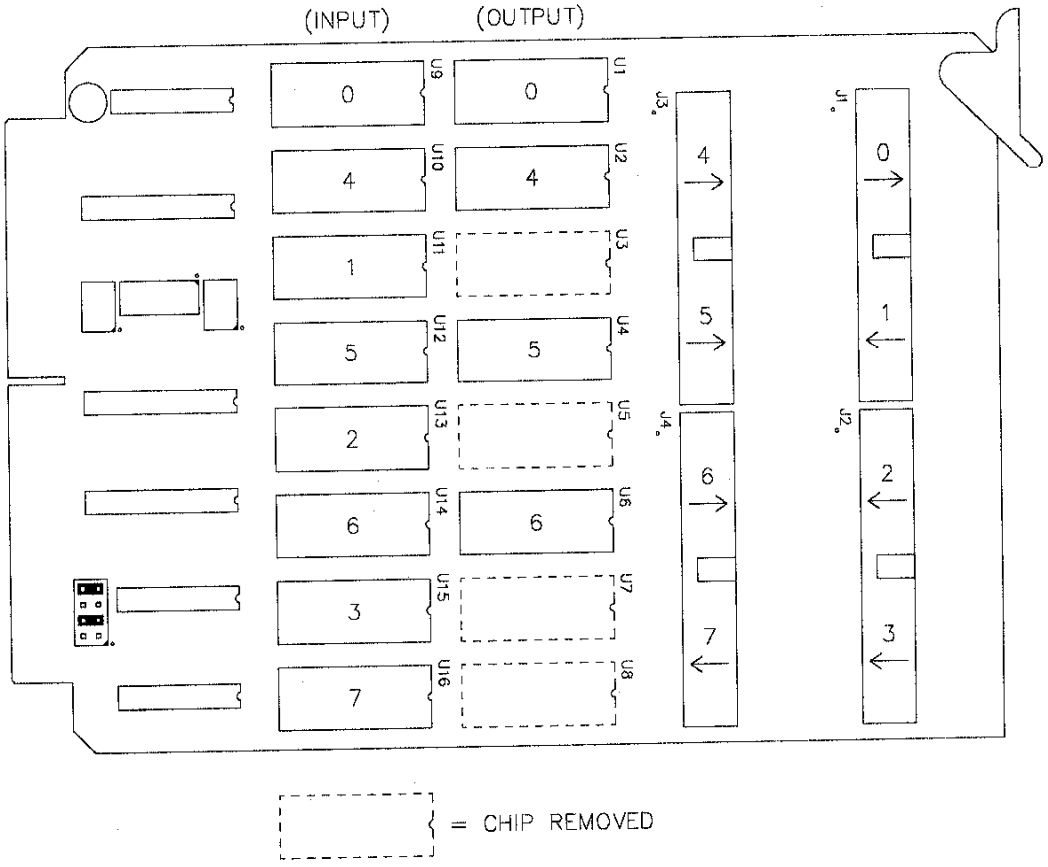


Figure 2-8. Typical I/O Configuration

Alternately the board can be configured as four ports (I/O addresses) with an input and an output channel at each location. This configuration is not recommended for most applications.

When this mode is used the the board must be configured only as shown below. Writing to channels 0 - 3 will output data on connectors J1 and J2. Reading channels 0 - 3 will input data from connectors J3 and J4.

This configuration does not allow for readback of output channel data.

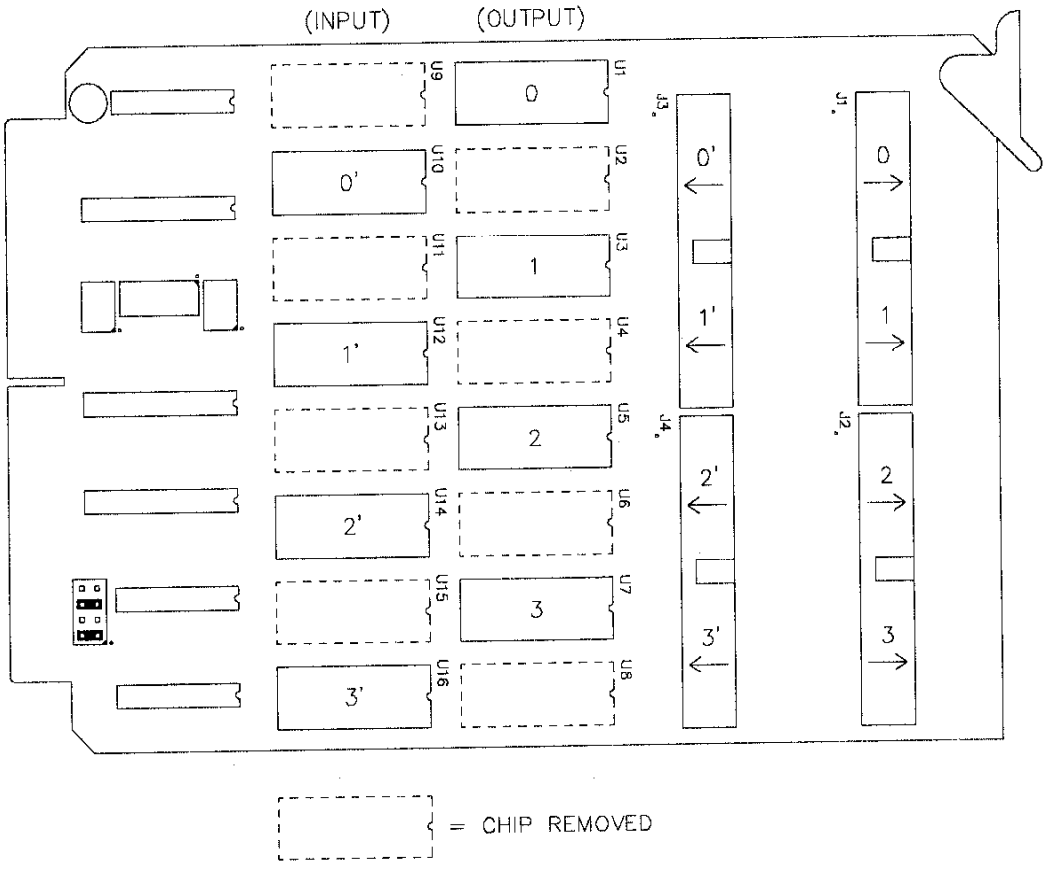


Figure 2-9. Special 4-Port Mode Configuration

Section 3
INSTALLATION

HANDLING

** CAUTION ** The VL-7614 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7614 card can be installed in any slot of an STD Bus card cage.

The VL-7614 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

** CAUTION ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** CAUTION ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connection to the VL-7614 can be made as noted below. Pinout listings for these connectors appear on the following pages. A pinout of the STD Bus connector appears in Section 5.

Connectors J1 - J4

Connectors J1 - J4 are 34-pin latching header type connectors (on .1" centers). They may each be connected to external equipment using mating connectors such as Ansley #609-3441, AMP #499506-0, and 3M #3414-6034. The mating connectors should include a strain relief in order to use the built-in latch bars.

Connector J1

Pin	Channel - Bit
1	0 - 0
3	0 - 1
5	0 - 2
7	0 - 3
9	0 - 4
11	0 - 5
13	0 - 6
15	0 - 7
17	1 - 0
19	1 - 1
21	1 - 2
23	1 - 3
25	1 - 4
27	1 - 5
29	1 - 6
31	1 - 7
33	Ground

2-34 even numbered pins ground.

Connector J2

Pin	Channel - Bit
1	2 - 0
3	2 - 1
5	2 - 2
7	2 - 3
9	2 - 4
11	2 - 5
13	2 - 6
15	2 - 7
17	3 - 0
19	3 - 1
21	3 - 2
23	3 - 3
25	3 - 4
27	3 - 5
29	3 - 6
31	3 - 7
33	Ground

2-34 even numbered pins ground.

Figure 3-1. Connectors J1 and J2 Pinouts

Connector J3

Pin	Channel - Bit
1	4 - 0
3	4 - 1
5	4 - 2
7	4 - 3
9	4 - 4
11	4 - 5
13	4 - 6
15	4 - 7
17	5 - 0
19	5 - 1
21	5 - 2
23	5 - 3
25	5 - 4
27	5 - 5
29	5 - 6
31	5 - 7
33	Ground

2-34 even numbered pins ground.

Connector J4

Pin	Channel - Bit
1	6 - 0
3	6 - 1
5	6 - 2
7	6 - 3
9	6 - 4
11	6 - 5
13	6 - 6
15	6 - 7
17	7 - 0
19	7 - 1
21	7 - 2
23	7 - 3
25	7 - 4
27	7 - 5
29	7 - 6
31	7 - 7
33	Ground

2-34 even numbered pins ground.

Figure 3-2. Connectors J3 and J4 Pinouts

Section 4
OPERATION

INTRODUCTION

This section includes general information about the use and operation of the VL-7614 card. It focuses primarily on the software commands necessary to operate the card and includes examples to assist you in constructing your own software routines.

I/O PORT MAPPING

The VL-7614 normally occupies eight I/O port addresses. Each I/O address corresponds to one 8-bit channel of inputs or outputs.

An alternate mapping may also be used which provides four ports that each access one input and one output channel. This mapping is not recommended for most applications and will not be covered in this section.

The locations of the eight ports is determined by the board address, which is jumper selectable. As shipped, the board is jumpered for hex address 00.

Once the board's I/O address has been determined, the addresses of the eight I/O ports can be determined as shown in Figure 4-1. Each I/O module port can be both read (for inputting data or reading the current output data) and written (for outputting data) depending on the physical configuration of the channel.

For applications that use byte-oriented data, each port can be read/written directly as needed. For applications that use bit-oriented data (i.e. many single status/control lines) the board is much easier to use with subroutines that treat it as 64 single addressable lines. Subroutines with this purpose are included later in this section.

Figure 4-2 details the way in which the bit numbering corresponds to each connector and port number (shown as shipped addressed at hex 00).

Port Address	Chan.#	Bit Number	Connector
Board Address + 0	0	0-7	J1
Board Address + 1	1	8-15	J1
Board Address + 2	2	16-23	J2
Board Address + 3	3	24-31	J2
Board Address + 4	4	32-39	J3
Board Address + 5	5	40-47	J3
Board Address + 6	6	48-56	J4
Board Address + 7	7	57-63	J4

Figure 4-1. I/O Port Locations

Conn.	Addr.	D7	D6	D5	D4	D3	D2	D1	D0
J1	00	7	6	5	4	3	2	1	0
J1	01	15	14	13	12	11	10	9	8
J2	02	23	22	21	20	19	18	17	16
J2	03	31	30	29	28	27	26	25	24
J3	04	39	38	37	36	35	34	33	32
J3	05	47	46	45	44	43	42	41	40
J4	06	55	54	53	52	51	50	49	48
J4	07	63	62	61	60	59	58	57	56

Figure 4-2. Bit Numbering

READING AND WRITING DATA

All of the I/O buffers on the VL-7614 board are non-inverting (to set an output pin low, write a zero, etc.).

Note that the data read always reflects the actual state of the I/O pin, even for output channels. If an I/O pin is shorted to ground it will always read as a zero. Writing a high or low bit to the pin (assuming it's an output channel) will have no effect on the data read.

All output channels are cleared (set low) at power-up and whenever a system reset occurs.

SOFTWARE EXAMPLES

Reading a VL-7614 port (data byte) is straightforward and requires no special considerations. If bit- oriented data is read, care must be taken to select the proper port and data bit which corresponds to the desired I/O line.

When writing to an I/O line, care must be taken not to change the current state of the seven other bits which appear at the same I/O port. This is easily done by reading the state of the output port before anding/oring in the bit that is being changed.

In systems where more than a few I/O lines are used, these operations can be made much easier with generalized subroutines that read or write to a specified I/O line. These subroutines calculate the port address and data bit involved and allow the programmer to concentrate on reading or writing to the desired line.

The routines allow reading of a single input line, writing to a single output line, and reading of a single output line to determine its current state.

The VL-7614 can be used with any language that allows direct access to system I/O ports. The examples below are shown in several programming languages. These examples have not necessarily been tested or verified for proper operation. They are supplied for general information only and may not be appropriate for any specific application.

Note: These routines use "readback" of the output channels. They assume (and require) that all the input buffer chips have been left in the board.

Assembly Language Examples

The following Z80 program fragments illustrate how the VL-7614 board can be used in an assembly language environment.

The first example illustrates direct access to each desired I/O line. This method is appropriate when byte-oriented data is read/written, or only a small number of I/O lines are connected to the interface. It requires that the programmer determine the related port and bit of the desired I/O line.

The second example illustrates access by I/O line number. It uses subroutines to read or write to a specified line, freeing the programmer from unnecessary calculations during program construction.

```
                    ;Example 1.  Direct access to the VL-7614.
                    ;
                    ;Define all port locations.
          0000      DIOBASE   EQU   00H             ;Board address = hex 00.
          0000      CHAN0     EQU   DIOBASE + 0     ;Channel 0 (lines 0-7).
          0001      CHAN1     EQU   DIOBASE + 1     ;Channel 1
          0002      CHAN2     EQU   DIOBASE + 2     ;Channel 2
          0003      CHAN3     EQU   DIOBASE + 3     ;Channel 3
          0004      CHAN4     EQU   DIOBASE + 4     ;Channel 4
          0005      CHAN5     EQU   DIOBASE + 5     ;Channel 5
          0006      CHAN6     EQU   DIOBASE + 6     ;Channel 6
          0007      CHAN7     EQU   DIOBASE + 7     ;Channel 7
          0008      CHAN8     EQU   DIOBASE + 8     ;Channel 8
                    ;
0100                     ORG       100H      ;Start of code.
                    ;
                    ;Reading a single line (state of input or output line).
0100    DB 00           IN  A,(CHAN0)    ;Read the I/O port.
0102    E6 02           AND 00000010B    ;Mask out all channels except #1.
0104    C2 08 01        JP  NZ,DOIT      ;Jump to somewhere if channel is ON.
0107    00                  NOP          ;Else do something here.
0108    00              DOIT    NOP      ;Dummy routine for jump above.
                    ;
                    ;
                    ;Setting a line ON (output pin high).
0109    DB 01           IN  A,(CHAN1)    ;Read the current state of the outputs.
010B    F6 40           OR  01000000B    ;Set the line #14 bit ON.
010D    D3 01           OUT (CHAN1),A    ;Write it to the board.
                    ;
                    ;
                    ;Setting a line OFF (output pin low).
010F    DB 02           IN  A,(CHAN2)    ;Read the current state of the outputs.
0111    E6 FB           AND 11111011B    ;Set the channel #18 bit OFF.
0113    D3 02           OUT (CHAN2),A    ;Write it to the port.
```

```
                    ;Example 2 - Accessing the VL-7614 by channel #.
                    ;
       0000         ADDR7614 EQU 00H          ;Board address = hex 00.
                    ;
0100                        ORG  100H         ;Start of code.
                    ;
                    ;reading an I/O line (state of input or output).
0100   3E 0C                LD   A,12         ;Specify line #12
0102   CD 14 01             CALL READ         ;Read it (result in A)
0105   C2 09 01             JP   NZ,DUMMY     ;Jump somewhere if it is ON.
0108   00                   NOP               ;(do something else if it isn't)
0109   00           DUMMY   NOP               ;(user routine)
                    ;
                    ;
                    ;Setting a line ON (output pin high).
010A   3E 09                LD   A,9          ;Specify line #9
010C   CD 1E 01             CALL ON           ;Turn it ON
                    ;
                    ;
                    ;Setting a line OFF (output pin low).
010F   3E 28                LD   A,40          ;Specify line #40
0111   CD 27 01             CALL OFF           ;Turn it OFF
                    ;
                    ;
                    ;** SUBROUTINES **
                    ;Reads a line (input or output). Chan.# (0-63) is in A.
                    ;Returns the state of the line (0 or 1) in reg. A.
0114   CD 33 01     READ    CALL FIND         ;Convert the line #.
0117   ED 78                IN   A,(C)        ;Read the port.
0119   A0                   AND  A,B          ;Mask for desired bit.
011A   C8                   RET  Z            ;Return if 0.
011B   3E 01                LD   A,1          ;Or else plug with a 1
011D   C9                   RET               ;and return.
                    ;
                    ;Sets an output line ON. Chan.# (0-63) is in reg. A.
011E   CD 33 01     ON      CALL FIND         ;Convert the line #.
0121   ED 78                IN   A,(C)        ;Read current output states.
0123   B0                   OR   B            ;Set line on.
0124   ED 79                OUT  (C),A        ;Write it to the port.
0126   C9                   RET               ;Return.
                    ;
                    ;Sets an output line off. Chan.# (0-63) is in reg. A.
0127   CD 33 01     OFF     CALL FIND         ;Convert the line #.
012A   78                   LD   A,B          ;Complement B (bit mask).
012B   2F                   CPL
012C   47                   LD   B,A
012D   ED 78                IN   A,(C)        ;Read current output states.
012F   A0                   AND  B            ;Set line off.
0130   ED 79                OUT  (C),A        ;Write it to the port.
0132   C9                   RET               ;Return
```

```
                        ;
                        ;Computes the port address and bit mask for the
                        ;requested line # (in register A).
                        ;Returns A=0, B=bit mask, C=port address
0133   3C       FIND    INC   A             ;Offset line # by 1.
0134   06 01           LD    B,1           ;Initialize B, for line #0.
0136   0E 00           LD    C,ADDR7614    ;Initialize C, for line #0.
0138   3D       L1      DEC   A             ;Decrement line #.
0139   C8              RET   Z             ;Done when A=0.
013A   CB 00           RLC   B             ;Rotate bit mask.
013C   30 FA           JR    NC,L1         ;Loop if no carry.
013E   0C              INC   C             ;Adjust port address.
013F   18 F7           JR    L1            ;Continue.
```

BASIC Language Examples

The subroutines and program fragments in the first listing below illustrate how the VL-7614 board can be used with standard BASICs (or other high level languages) that include logical AND, OR, and XOR functions. Microsoft's BASIC-80 is used in this example.

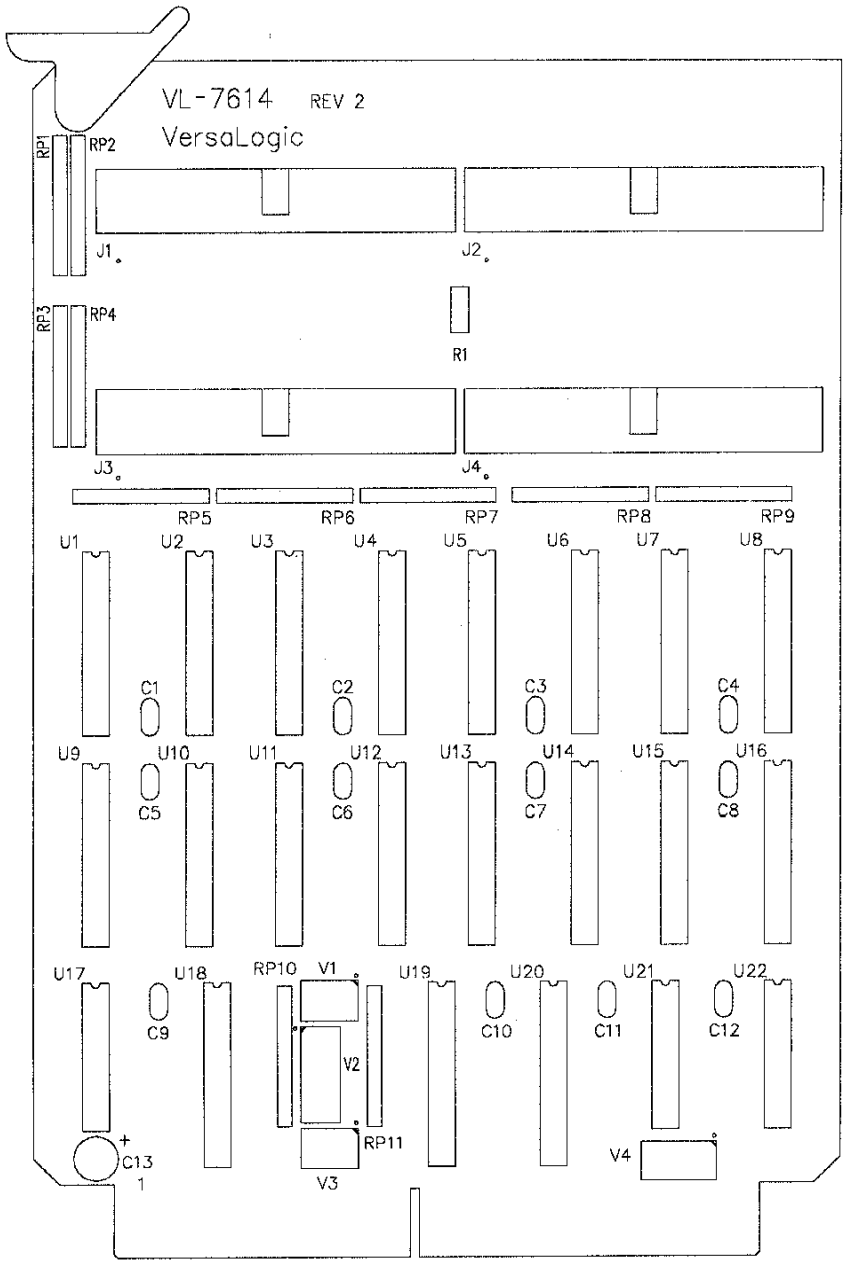
Users of VersaLogic's C4 BASIC language should refer to the second listing which shows these same functions written in C4 BASIC.

Note: These routines may not operate correctly with some BASICs or be suitable for your application.

```
10 REM Microsoft BASIC-80 language example for the VL-7614 board.
20 REM To read or write to single I/O lines (#0-63).
30 REM
50 REM Set address of Digital Interface (DI) board (00 hex = 00 decimal)
51 DI = 0
 .
 .
100 REM Read line 0 and do something if it's ON.
110 LINE=0: GOSUB 510
120 IF STATE = 1 THEN GOTO 1000
 .
 .
150 REM Turn ON line 11
155 LINE=11: GOSUB 570
 .
 .
170 REM Turn line 8 OFF
171 LINE=8: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7614 BOARD.
501 REM These routines are called with the line # (0-63) in "LINE".
502 REM Input data is returned in "STATE" (1=ON, 0=OFF).

510 REM Read the line in "LINE" (0-63)
520 GOSUB 600 : STATE=INP(ADDR) AND MASK : IF STATE > 0 THEN STATE=1
530 RETURN

540 REM Turn OFF line "LINE" (0-63)
550 GOSUB 600 : OUT ADDR,(INP(ADDR) AND (255 XOR MASK)
560 RETURN

570 REM Turn ON line "LINE" (0-63)
580 GOSUB 600 : OUT ADDR,(INP(ADDR) OR MASK))
590 RETURN

600 REM Computes port address and bit mast for routines above.
610 X=INT(LINE/8) : ADDR=DI+X : MASK=2^(LINE-8*X) : RETURN
```

```
10 REM VersaLogic C4 BASIC language example for the VL-7614 board.
20
50 REM Set address of Digital Interface (D1) board (00 hex)
51 D1 = &00
 .
 .
100 REM Read line 0 and do something if it's ON.
110 N=0: GOSUB 510
120 IF S = 1 GOTO 1000
 .
 .
150 REM Turn ON line 11
155 N=11: GOSUB 570
 .
 .
170 REM Turn line 31 OFF.
171 N=31: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7614 BOARD.
501 REM These routines are called with the line # in "N" (0-63).
502 REM Input data is returned in "S" (1=ON, 0=OFF).

510 REM Read the line in "N"
520 GOSUB 595 : S=IN(X) AND X1 : If S>0 S=1
530 RETURN

540 REM Turn OFF line "N"
550 GOSUB 595 : OUT X,(IN(X) AND NOT (X1))
560 RETURN

570 REM Turn ON line "N"
580 GOSUB 595 : OUT X,(IN(X) OR X1)
590 RETURN

594 REM Computes port addr (X) and bit mask (X1) for routines above
595 X=(N/8)+D1 : X1=1: X2=MOD(N,8): IF X2=0 RETURN
596 FOR X3 = 1 TO X2 : X1=X1*2 : NEXT X3 : RETURN
```

VL-7614 REV 2 Parts Placement Diagram 09/04/91



VL-7614 REV 2

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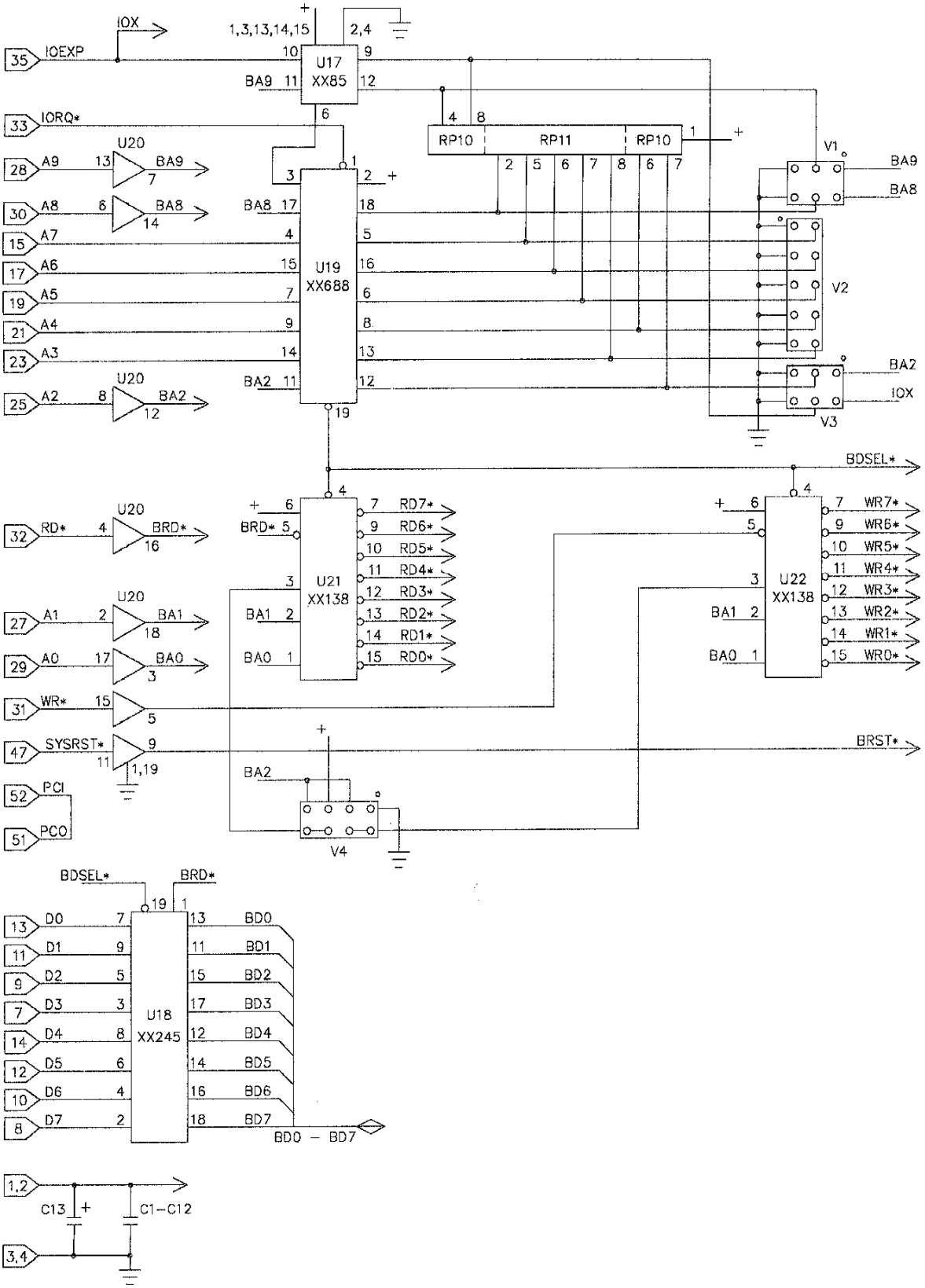

VL-7614 REV 2

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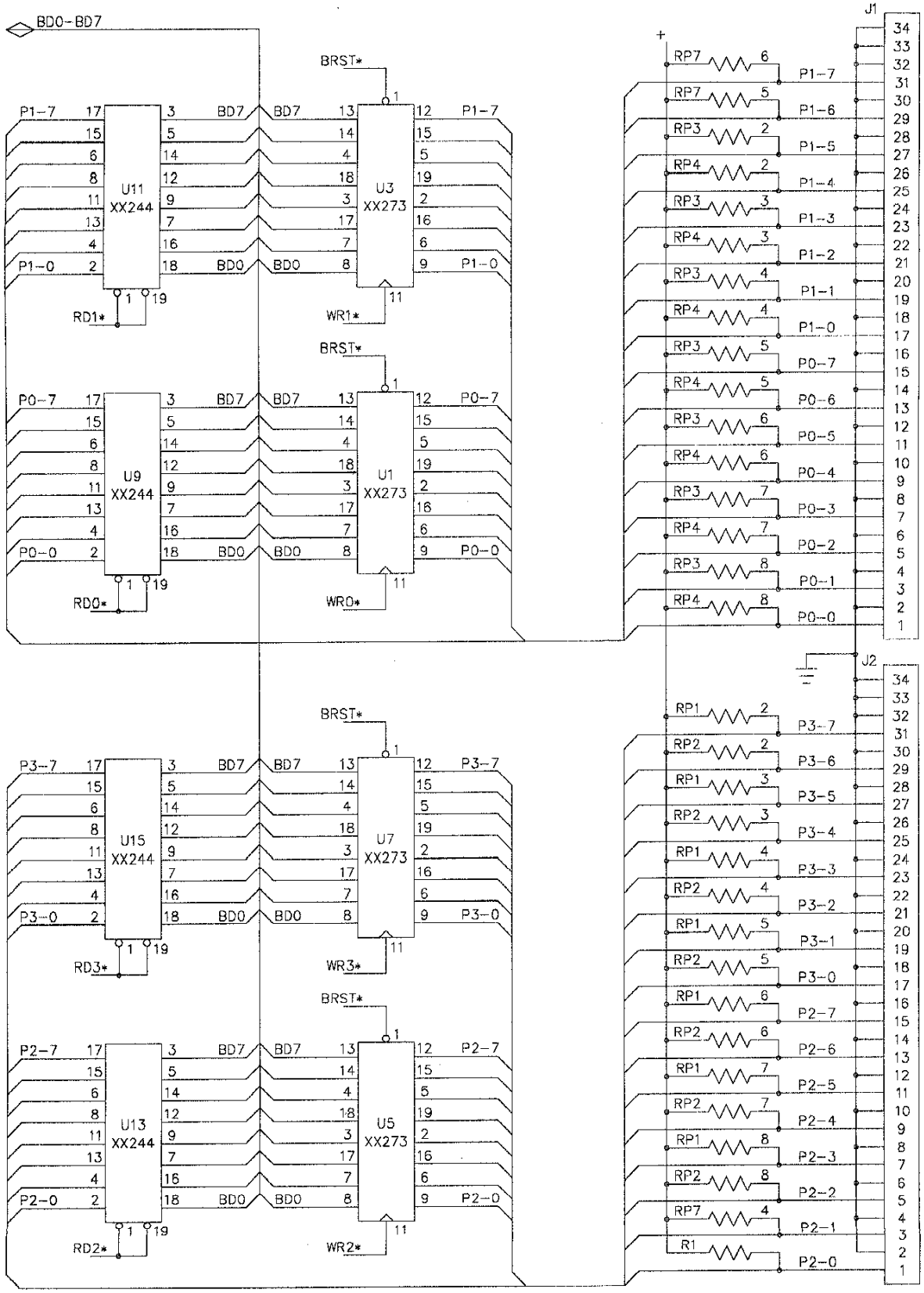

VL-7614 REV 2

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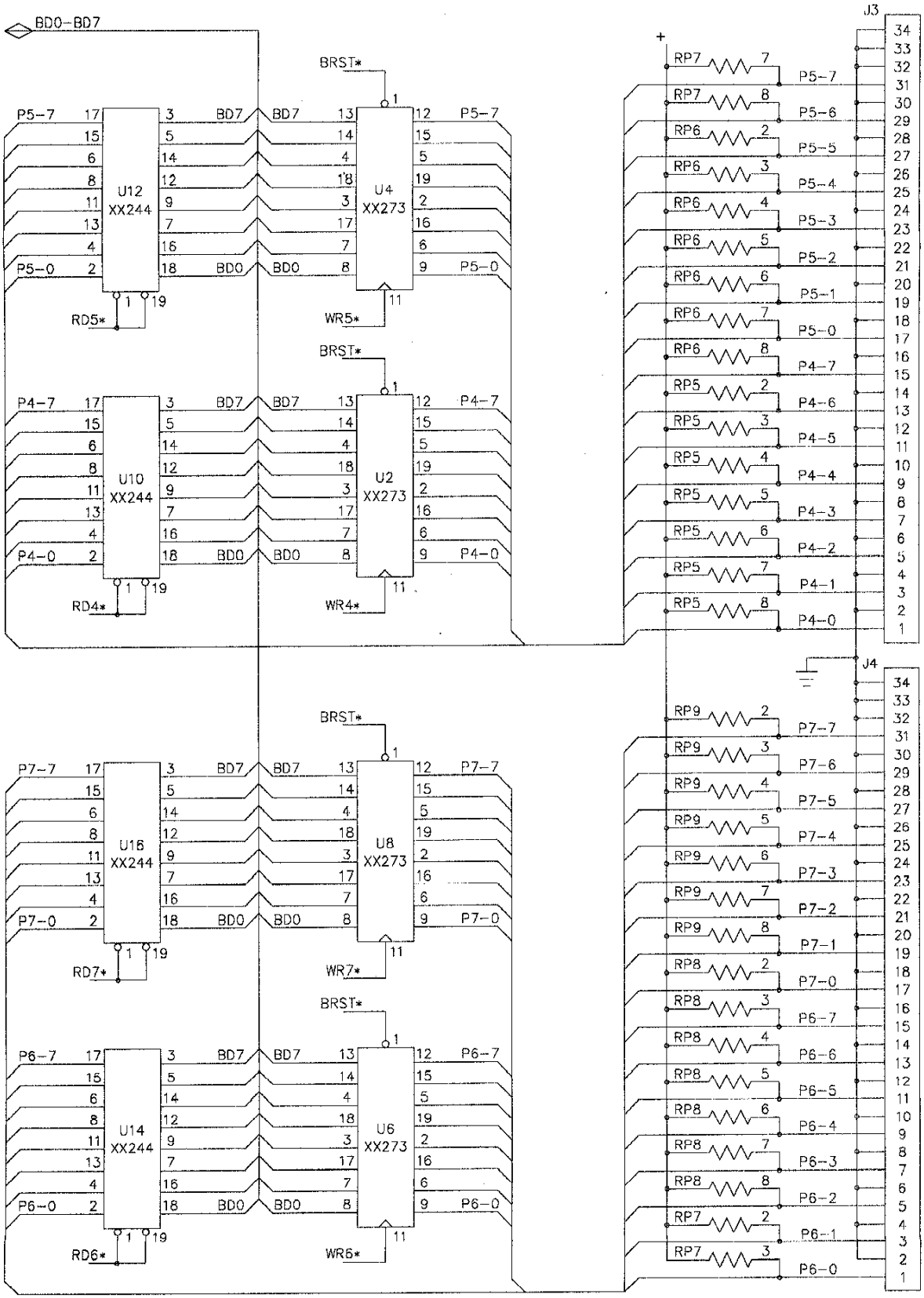

VL-7614 PARTS LIST
64 Line TTL Interface

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	74LS273
U9-U16, U20	74LS244
U17	74LS85
U18	74LS245
U19	74HCT688
U21, U22	74LS138

Resistors

R1	4K7 ohm, 5%, 1/4 W
RP1-RP9	4K7 ohm, 7 resistor SIP
RP10, RP11	10K ohm, 7 resistor SIP

Miscellaneous

J1, J2, J3, J4	34 pin R/A latching header

VL-76CT14 PARTS LIST
64 Line TTL Interface (Extended Temperature Version)

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	74HCT273
U9-U16, U20	74ACT244
U17	74HCT85
U18	74ACT245
U19	74HCT688
U21, U22	74HCT138

Resistors

R1	10K ohm, 5%, 1/4 W
RP1-RP9	10K ohm, 7 resistor SIP
RP10, RP11	100K ohm, 7 resistor SIP

Miscellaneous

J1, J2, J3, J4	34 pin R/A latching header

STD BUS PINOUT

Connections from the VL-7614 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7614.

COMPONENT SIDE				SOLDER SIDE			
PIN	SIGNAL	FLOW	DESCRIPTION	PIN	SIGNAL	FLOW	DESCRIPTION
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3/A19	I/O	Data bus	8	D7	I/O	Data bus
9	D2/A18	I/O	Data bus	10	D6	I/O	Data bus
11	D1/A17	I/O	Data bus	12	D5/A21	I/O	Data bus
13	D0/A16	I/O	Data bus	14	D4/A20	I/O	Data bus
15	A7	In	Address bus	16	A15	-	Address bus
17	A6	In	Address bus	18	A14	-	Address bus
19	A5	In	Address bus	20	A13	-	Address bus
21	A4	In	Address bus	22	A12	-	Address bus
23	A3	In	Address bus	24	A11	-	Address bus
25	A2	In	Address bus	26	A10	-	Address bus
27	A1	In	Address bus	28	A9	In	Address bus
29	A0	In	Address bus	30	A8	In	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	-	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	-	Memory expansion
37	REFRESH*	-	Refresh timing	38	MCSYNC*	-	Machine cycle sync.
39	STATUS1*	-	CPU status	40	STATUS0*	-	CPU status
41	BUSAK*	-	Bus acknowledge	42	BUSRQ*	-	Bus request
43	INTAK*	-	Interrupt acknowl.	44	INTRQ*	-	Interrupt request
45	WAITRQ*	-	Wait request	46	NMIRQ*	-	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	-	Push button reset
49	CLOCK*	-	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	-	±12 volt ground	54	AUXGND	-	±12 volt ground
55	AUX+V	-	+12 volt input	56	AUX-V	-	-12 volt input

Notes:
* Denotes an active low signal.

DECIMAL / HEX / ASCII CONVERSION CHART

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol denotes control characters. "^A" represents control A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20		64	40	@	96	60	`
1	01	^A SOH	33	21	!	65	41	A	97	61	a
2	02	^B STX	34	22	"	66	42	B	98	62	b
3	03	^C ETX	35	23	#	67	43	C	99	63	c
4	04	^D EOT	36	24	$	68	44	D	100	64	d
5	05	^E ENQ	37	25	%	69	45	E	101	65	e
6	06	^F ACK	38	26	&	70	46	F	102	66	f
7	07	^G BEL	39	27	'	71	47	G	103	67	g
8	08	^H BS	40	28	(	72	48	H	104	68	h
9	09	^I HT	41	29	)	73	49	I	105	69	i
10	0A	^J LF	42	2A	*	74	4A	J	106	6A	j
11	0B	^K VT	43	2B	+	75	4B	K	107	6B	k
12	0C	^L FF	44	2C	,	76	4C	L	108	6C	l
13	0D	^M CR	45	2D	-	77	4D	M	109	6D	m
14	0E	^N SO	46	2E	.	78	4E	N	110	6E	n
15	0F	^O SI	47	2F	/	79	4F	O	111	6F	o
16	10	^P DLE	48	30	0	80	50	P	112	70	p
17	11	^Q DC1	49	31	1	81	51	Q	113	71	q
18	12	^R DC2	50	32	2	82	52	R	114	72	r
19	13	^S DC3	51	33	3	83	53	S	115	73	s
20	14	^T DC4	52	34	4	84	54	T	116	74	t
21	15	^U NAK	53	35	5	85	55	U	117	75	u
22	16	^V SYN	54	36	6	86	56	V	118	76	v
23	17	^W ETB	55	37	7	87	57	W	119	77	w
24	18	^X CAN	56	38	8	88	58	X	120	78	x
25	19	^Y EM	57	39	9	89	59	Y	121	79	y
26	1A	^Z SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL