VL-EPMp-34 WILDCAT CMOS SETUP PARAMETERS

This article provides reference information and tips for setting CMOS Setup parameters on the VL-EPMp-34 (Wildcat). Start CMOS Setup by pressing Delete during the early boot cycle. The Main menu appears first. You can scroll to other menus using the left and right arrow keys. The CMOS Setup menus are:

Main	Exit	Boot	POST	SIO	Features
Firmbase	Misc	Video	Chipset	Board	AdvancedCPU

The basic idea when using CMOS Setup is to navigate to the menus containing fields you want to review, and change those fields as desired. When your settings are complete, navigate to the Exit menu, and select “Save Settings and Restart.” This causes the settings to be stored in nonvolatile memory in the system, and the system will reboot so that POST can configure itself with the new settings. After rebooting it may be desirable to reenter the Setup system as necessary to adjust settings as necessary.

Once the system boots, CMOS Setup cannot be entered; this is because the memory used by the BIOS configuration manager is deallocated by the system BIOS, so that it can be used by the OS when it boots. To reenter CMOS Setup after boot, simply reset the system or power off and power back on.

Note: The configurations and factory defaults described here are for VL-EPMp-34 BIOS version 6.5.103.

Main Menu

The Main menu displays the main system components and allows editing of the date and time.

```
+ ------------------------ ---------------------------- + ------------------
- +
| System Summary                                        |Use TAB to switch
|
| ------------------------ ---------------------------- |between month, day
|
| Phoenix[R] System BIOS                                |and year.  Use
digits|
| VersaLogic Version    6.5.103                         |and BKSP to change
|
| Core Version          EB(SF).005                      |field.
|
| BIOS Build Date       04/21/11                        |
|
| System BIOS Size      128KB                           |
|
| CPM/CSPM/BPM Modules  P7C7, GM45, EPMp34              |
|
| StrongFrame[R] Technology, Firmbase(R) Technology     |
|
```

```
|                                                                  |
|
| Processor (CPU)                                                  |
|
| Intel(R) Core(TM)2 Duo          P9300   @ 2.26GHz                |
|
| Processor Count       2                                          |
|
|                                                                  |
|
| System Memory (RAM)                                              |
|
| Low Memory (KB)       626                                        |
|
| Extended Memory (KB)  2052928                                    |
|
| Memory Above 4GB      0                                          |
|
|                                                                  |
|
| Real Time Clock (RTC)                                            |
|
| RTC Date              [04/21/2011]                               |
|
| RTC Time              [01:04:15]                                 |
|
+ ------------------------- -------------------------- + ----------------
- +
```

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RTC Date
RTC Time

The real time clock (RTC) date is factory set to the date of the BIOS build. The date and time are editable.

Exit Menu

The Exit menu allows you to save or discard changes and exit, or restore default settings and exit.

```
+ ------------------------- -------------------------- + ----------------
- +
| Save, Restore, and Exit Setup                        |Press ENTER to save
|
| ------------------------- -------------------------- |changes and reboot
|
| Save Settings and Restart            [Enter]         |system.
|
|                                                      |
|
| Exit Setup Without Saving Changes    [Enter]         |
|
```

```
|                                                          |
|
| Reload Factory-Defaults and Restart  [Enter]             |
|
|                                                          |
|
| Reload Custom-Defaults and Restart   [Enter]             |
|
|                                                          |
|
+ ------------------------- --------------------------- + ------------------
- +
```

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You can exit CMOS Setup by selecting one of the options below. To select an option, position the cursor over the option and press Enter. Pressing Esc at any time in CMOS Setup is equivalent to "Exit Setup Without Saving Changes."

- **Save Settings and Restart:** Saves all changes made to CMOS settings and reboots the VL-EPMp-34.
- **Exit Setup Without Saving Changes:** Does not save any changes made to CMOS settings and continues with POST as normal.
- **Reload Factory-Defaults and Restart:** Resets CMOS to factory defaults, even if there are custom defaults available. All changes made to CMOS settings during the current and previous CMOS Setup sessions will revert.
- **Reload Custom-Defaults and Restart:** Resets CMOS to custom defaults. Use the Flash BIOS Update (FBU) utility to save custom defaults.

Boot Menu

The Boot menu configures boot actions and devices.

```
+ ------------------------- --------------------------- + ------------------
- +
| System Boot Configuration                            |Select
initialization|
| ------------------------- --------------------------- |and boot priority
for|
|                                                      |all devices.
|
| Boot Device Prioritization (BBS)                     |
|
| 0 [SATA JN5_Top]                                     |Backspace deletes
|
| 1 [SATA JN5_Bot]                                     |selection. Space
|
| 2 [None]                                             |bar, + and - change
|
|                                                      |selections.
|
```

```
| Initialization Policy [All Devices]                    |
|                                                        |
|                                                        |
|                                                        |
| IDE Drive Configuration                                |
|                                                        |
|                                                        |
|                                                        |
| ICH ATA Controller Configuration                       |
|                                                        |
| ------------------------- -------------------------- |
|                                                        |
| SATA Controller               [Native Mode]            |
|                                                        |
|                                                        |
|                                                        |
+ ------------------------- -------------------------- + ------------------
- +
```

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Boot Device Prioritization (BBS)

Values: SATA JN5_Top, SATA JN5_Bot, Enter BIOS Preeboot Screen, Enter BIOS Setup Screen, Reboot System, PCI Slot 1-4, 82541, IBA GE Slot 0100 v1338 card in On-board ..., All other devices, USB Floppy, USB Hard Drive 0-8, USB CDROM Drive, None

Lists the devices and activities to be performed in the order in which they appear in the list -- the BIOS boot specification (BBS). When the BIOS completes POST, it follows this list, attempting to process each item. Some items are drives, such as an IDE drive, or a USB hard disk, or CDROM.

The ordering of the drives in the BBS list controls the BIOS in several ways. First, it is the list of drives that is scanned and assigned BIOS unit numbers for DOS (0, 1, 2 for floppy-type devices, and 80h, 81h, 83h, and so on for hard drives). If a drive on the list is not plugged in or working properly, the BIOS moves on to the next drive, skipping the inoperative one. Second, once the drives in the list have been verified, POST attempts to boot from them in that order as well. Drives without bootable partitions might be configured, but skipped over in the boot phase, so that other drives on the list become candidates for booting the OS.

The BBS list also contains other boot actions, such as boot from network cards and PCI slots, as well as special BIOS boot actions. When deciding what boot action to do first and then next in succession, POST first scans all the drives in the list to verify they are present and operating properly, and then goes down the list and tries to perform the actions in order. During this boot phase, if the list item is a drive, an attempt is made to boot from the boot record of that drive. If the list item is a device like a network card or PCI slot, an attempt is made to boot from that device. If the list item is a software item like “Enter BIOS Preboot Screen,” then it performs that action, and when that action completes, it moves on to the next item in the BBS list.

If detected, the names and serial numbers of drives connected to the board will appear after the connector number.

Initialization Policy

Values: All Devices, Boot Devices Only

Specifies the policy used to determine if device specific initialization code should be executed. Boot Devices Only prevents the initialization of devices not assigned a boot priority.

SATA Controller

Values: Native Mode, AHCI Mode, Disable, Compatible Mode

Enables or disables the SATA controller and selects its mode. Changes to this setting require saving CMOS settings and rebooting before the boot menu updates.

POST Menu

The POST menu configures power-on self-test settings.

```
+ ------------------------- --------------------------- + ------------------
- +
| POST Memory Tests                                     |Enable basic memory
|
| ------------------------- --------------------------- |confidence test
below|
| Low Memory Standard Test     [Enabled]                |1MB during POST.
|
| Low Memory Exhaustive Test   [Disabled]               |
|
| High Memory Standard Test    [Disabled]               |
|
| High Memory Exhaustive Test  [Disabled]               |
|
| Click During Memory Test     [Enabled]                |
|
| Clear Memory During Test     [Disabled]               |
|
|                                                       |
|
| POST Error Control                                    |
|
| ------------------------- --------------------------- |
|
|                                                       |
|
| POST User Interface                                   |
|
| ------------------------- --------------------------- |
|
```

```
| POST Display Messages        [Enabled]                  |
|
| POST Operator Prompt         [Enabled]                  |
|
| POST Display PCI Devices     [Enabled]                  |
|
|                                                         |
|
| POST Debugging                                          |
|
| ------------------------- --------------------------- |
|
| POST Slow Reboot Cycle       [Disabled]                 |
|
| POST Fast Reboot Cycle       [Disabled]                 |
|
|                                                         |
|
| Device Initialization                                   |
|
| ------------------------- --------------------------- |
|
| POST Floppy Seek             [Disabled]                 |
|
| POST Hard Disk Seek          [Enabled]                  |
|
+ ------------------------- --------------------------- + ------------------
- +
```

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POST Memory Tests

Enables or disables the following memory tests during POST:

- **Low Memory Standard Test:** Basic confidence test of memory below the 1 MB address boundary (conventional memory, or memory normally used by DOS).
- **Low Memory Exhaustive Test :** Exhaustive confidence test of memory below 1 MB.
- **High Memory Standard Test:** Basic confidence test of memory above the 1 MB address boundary.
- **High Memory Exhaustive Test:** Exhaustive confidence test of memory above 1 MB.
- **Click During Memory Test:** Audible click after each tested memory block.
- **Clear Memory During Test:** Sets all memory locations tested to 0. This is required only for some legacy DOS programs that might rely on cleared memory to operate properly.

POST User Interface

Enables or disables the following POST messaging:

- **POST Display Messages:** Text messages displayed during POST. When disabled, POST is "quiet."
- **POST Operator Prompt:** Operator prompts if POST is configured to ask interactive questions of the user about whether to use specific features.
- **POST Display PCI Devices:** Display of PCI devices.

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POST Debugging

Enables or disables slow or fast reboot cycles for diagnostic purposes.

- **POST Slow Reboot Cycle:** The system reboots late in POST. Used to exercise system memory and peripherals without requiring a boot to an operating system.
- **POST Fast Reboot Cycle:** The system reboots repeatedly early in POST. Used to verify that the system can reboot quickly many times in succession.

Device Initialization

Enables or disables floppy drive or hard disk seek during POST for diagnostic purposes.

- **POST Floppy Seek:** Executes a head seek on each floppy drive connected to the system. Used to recalibrate the drive in some systems with older DOS operating systems.
- **POST Hard Disk Seek:** Executes a head seek on each hard drive connected to the system. This extends the standard test performed on each drive by requesting that the drive actually move the head.

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SIO Menu

The SIO menu configures super I/O devices, such as serial and parallel ports. Note that the default addresses assigned to the serial ports are not the only ones possible, but they do ensure compatibility with legacy software, especially early DOS programs that do not use the BIOS to access the ports.

```
+ ------------------------ -------------------------- + ------------------
- +
| BIOS Super I/O Configuration                        | RS-422/485/232-
4wire|
| ------------------------ -------------------------- | on JN2, CBR-3406.
|
|                                                     |
|
| SMSC LPC47N217 (North Board) Devices                |
|
```

```
| ------------------------- ---------------------------- |
|
| Serial Port 5                  [Enabled]                 |
|
|   Address                      [220h]                    |
|
|   IRQ                          [IRQ 5]                   |
|
|   Mode                         [RS-232 (4-wire)]         |
|
|                                                          |
|
| SMSC SCH3114 (South Board) Devices                       |
|
| ------------------------- ---------------------------- |
|
| Daniels board not installed.                             |
|
|                                                          |
|
+ ------------------------- ---------------------------- + ------------------
- +
```

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Serial Port 5

Enables or disables COM ports and sets port addresses, interrupts, and modes.

- **Address:** 3f8h, 2f8h, 3e8h, 2e8h, 220h, 228h, 238h, 338h
- **IRQ:** IRQ 3, IRQ 4, IRQ 5, IRQ 7, IRQ 10, No IRQ
- **Mode:** RS-232 (4-wire), RS-422, RS-485 (Manual/DTR flow control)

Because the COM ports are ISA devices, and IRQs cannot be shared with devices (including other COM ports) on the ISA bus, you must assign independent IRQs to these ports, or disable them if not needed. Make sure you don't assign an IRQ used by a PCI interrupt.

Mode notes:

- RS-232 (4-wire): Only the TX, RX, CTS, and RTS signals are used. This will work for terminal communication, but not for a modem.

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Features Menu

The Features menu enables and disables system BIOS features and configures console redirection and CPU settings.

```
+ ------------------------- ---------------------------- + ------------------
- +
```

```
| BIOS Feature Configuration                                  |Enable to
initialize |
| -------------------------- ---------------------------- |APICs and use them
in|
| Interrupt Processing           [Use APIC]                |an emulated PIC
mode.|
| MP Tables (non ACPI OSes)      [Enabled]                 |If you wish to use
|
| Quick Boot                     [Enabled]                 |full-APIC mode,
this |
| ACPI                           [Enabled]                 |must be set AND
|
| POST Memory Manager            [Enabled]                 |either ACPI or MP
|
| System Management BIOS         [Enabled]                 |must be enabled. DO
|
| Splash Screen                  [Disabled]                |NOT CHANGE AFTER OS
|
|                                                          |INSTALL.
|
| Console Redirection                                      |
|
| -------------------------- ---------------------------- |
|
| Use Console Assignments Below [On Remote User Detect]    |
|
| POST Console                   [COM1]                    |
|
|                                                          |
|
| Legacy Free Option                                       |
|
| -------------------------- ---------------------------- |
|
| Legacy-Free                    [Disabled]                |
|
| ACPI FACP 8042 Flag            [Disabled]                |
|
|                                                          |
|
| Plug-n-Play (PnP) Configuration                          |
|
| -------------------------- ---------------------------- |
|
| Plug-n-Play                    [Enabled]                 |
|
|                                                          |
|
+ -------------------------- ---------------------------- + ------------------
- +
```

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Interrupt Processing

Values: Use APIC, Use Legacy PIC

Initializes APICs and uses them in an emulated PIC mode. For full-APIC mode, this parameter must be enabled along with ACPI. Do not change this setting after an operating system has been installed.

MP Tables (non ACPI OSes)

Values: Enabled, Disabled

Enabling this feature provides operating systems with APIC and processor information according to the Multi-Processor Specification. This feature requires the use of APICs. Do not change this setting after an operating system is installed.

Quick Boot

Values: Enabled, Disabled

Enables or disables a time-optimized POST, causing preconfigured boot optimizations to be made when the system boots. This will reduce POST time.

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ACPI

Values: Enabled, Disabled

Advanced control and power management (ACPI) is used with ACPI-aware operating systems. Do not change this setting after installing the OS.

POST Memory Manager

Values: Enabled, Disabled

Enables or disables the POST memory manager, which is needed by the preboot execution environment (PXE) boot ROMs to allocate memory for POST-time operation in order to perform their functions. If your boot ROM supports PXE, then you should enable this option.

System Management BIOS

Values: Enabled, Disabled

Enables or disables System Management BIOS, which supports DMI agents and other PXE clients.

Splash Screen

Values: Enabled, Disabled

Enables or disables the display of the splash screen during the boot cycle. When the splash screen is enabled, it appears on the computer display for approximately one second. To learn how to create a custom splash screen, see VT1400 How to Create a Splash Screen.

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Use Console Assignments Below

Values: On Remote User Detect, Always, Never

When set to Always, the console is directed to the selected device. When set to On Remote User Detect, the console will be directed to the selected device only when there is no video device available, or when the user has specifically requested redirection by pressing Enter or Ctrl-C on the serial terminal. CMOS Setup and some operating systems such as DOS can use the redirected console for user interaction. The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control. (See "Console Redirection" in the *VL-EPMp-34 Reference Manual*.)

POST Console

Values: COM1, COM2, None

Sets the serial port for console redirection.

Note: The Preboot Console and Debugger Console parameters are not used.

Legacy-Free

Values: Enabled, Disabled

Enables or disables support for Microsoft's Legacy-Free Specification.

ACPI FACP 8042 Flag

Values: Enabled, Disabled

Enables or disables the 8042 bit in the Boot Architecture Flags. Operating systems may interepret this in different ways that affect rebooting and legacy device detection.

Plug-N-Play

Values: Enabled, Disabled

Enables or disables Plug-n-Play 1.0A specification support. When enabled, system device nodes are created for legacy ISA and PCI devices, but no automatic ISA resource management is performed.

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Firmbase Menu

The Firmbase menu configures Firmbase Technology (the 32-bit firmware infrastructure of the BIOS). It is recommended that you do not change settings beyond the Basic Firmbase Technology Configuration options on this menu.

```
+ ------------------------ -------------------------- + ------------------
- +
| Features Enabled by Firmbase[R] Technology            |Enable to support
USB|
| ------------------------ -------------------------- |keyboard and mouse
|
| Legacy USB                    [Enabled]               |
|
| USB Boot                      [Enabled]               |
|
| EHCI/USB 2.0                  [Disabled]              |
|
| Firmbase User Shell           [Enabled]               |
|
|                                                       |
|
| Basic Firmbase[R] Technology Configuration            |
|
| ------------------------ -------------------------- |
|
| Firmbase Technology           [Enabled]               |
|
| Periodic SMI                  [Enabled]               |
|
| Firmbase Debug Log            [None]                  |
|
| Firmbase System Console       [None]                  |
|
| Firmbase Shell on Serial Port [None]                  |
|
|                                                       |
|
| Firmbase[R] Technology Foreground IRQ Monitoring      |
|
| ------------------------ --------------------------|
|
| IRQ0 (Timer)                  [Disabled]              |
|
| IRQ1 (Keyboard)               [Disabled]              |
|
| IRQ2 (Cascade)                [Disabled]              |
|
| IRQ3 (COM2/COM4)              [Disabled]              |
|
| IRQ4 (COM1/COM3)              [Disabled]              |
|
| IRQ5 (LPT2)                   [Disabled]              |
|
```

```
| IRQ6 (Floppy)                 [Disabled]              |
|
| IRQ7 (LPT1)                   [Disabled]              |
|
| IRQ8 (RTC)                    [Disabled]              |
|
| IRQ9 (PCI/SCI)                [Disabled]              |
|
| IRQ10 (PCI)                   [Disabled]              |
|
| IRQ11 (PCI)                   [Disabled]              |
|
| IRQ12 (Mouse)                 [Disabled]              |
|
| IRQ13 (NPX)                   [Disabled]              |
|
| IRQ14 (IDE)                   [Disabled]              |
|
| IRQ15 (IDE)                   [Disabled]              |
|
|                                                       |
|
+ -------------------------- ---------------------------- + ------------------
- +
```

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Legacy USB

Values: Disable, Enable

Enables or disables BIOS support for USB keyboards and USB mice.

USB Boot

Values: Enabled, Disabled

Enables BIOS access to USB mass storage devices. The Enabled setting is required for booting from USB hard drives or CD-ROM drives. It is not required for the OS access to USB mass storage devices.

EHCI/USB 2.0

Values: Enabled, Disabled

The BIOS is capable of booting from a USB device, or of mounting one as a drive letter. If EHCI/USB 2.0 is enabled, this access will take advantage of the USB 2.0 (EHCI) controller. Otherwise, the USB 1.1 (OHCI) controller will be used. In either case, the EHCI controller is available for the OS to use.

Firmbase User Shell

Values: Enabled, Disabled

Enables or disables the Firmbase shell.

Firmbase Technology

Values: Enabled, Disabled

Enables or disables Firmbase Technology. Set to Enable to provide SMM support for legacy USB, USB booting, and some other features.

Periodic SMI

Values: Enabled, Disabled

Enables or disables the periodic System Management Interrupt. Enabling this option gives periodic CPU time slices to Firmbase after POST completes. Firmbase primarily allows USB keyboards and mass storage devices to behave as legacy PS/2 and IDE devices for operating systems such as DOS, which don't natively support USB. Disabling this option can improve reliability of serial port traffic running at 115200 baud or greater. It should also be disabled for real-time applications with latency sensitivity in the 1 millisecond range.

Firmbase Debug Log

Values: None, COM1, COM2, COM3, COM4

Specifies the device used to display diagnostic messages for Firmbase.

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Firmbase System Console

Values: None, COM1, COM2, COM3, COM4

Specifies the device used by the Firmbase system process to display sign-on banners of all Firmbase applications loaded during system initialization.

Firmbase Shell on Serial Port

Values: None, COM1, COM2, COM3, COM4

Specifies a serial port that can be used by the Firmbase command line interpreter as an extra user session. This is useful in configurations without a keyboard or monitor to support virtual consoles.

Firmbase Technology Foreground IRQ Monitoring

Values: Enabled, Disabled

Enables or disables foreground IRQ monitoring for specific interrupts. If a monitored IRQ is pending while Firmbase is running, then control will be quickly returned to the foreground OS where the IRQ can be serviced. This can help some latency-sensitive applications.

BACK TO FIRMBASE

Misc Menu

The Misc menu configures miscellaneous features such as system cache and keyboard control.

```
+ ------------------------- ---------------------------- + ------------------
- +
| Cache Control                                          |Enable to allow CPU
|
| ------------------------- ---------------------------- |caching to operate.
|
| System Cache                  [Enabled]                |
|
|                                                        |
|
| Keyboard Control                                       |
|
| ------------------------- ---------------------------- |
|
| Keyboard Numlock LED          [Disabled]               |
|
| Typematic Rate                [30/sec]                 |
|
| Typematic Delay               [250ms]                  |
|
|                                                        |
|
|                                                        |
|
+ ------------------------- ---------------------------- + ------------------
- +
```

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System Cache

Values: Enabled, Disabled

Enables or disables the operation of L2 cache.

Keyboard NumLock LED

Values: Enabled, Disabled

Enables or disables NumLock. Set this option to Disabled to turn off the NumLock key when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. Some operating systems, such as DOS, honor this initial setting and use it for run-

time operations. Other operating systems, such as Windows, assume complete control of the NumLock state, and do not honor this setting.

BACK TO MISC

Typematic Rate

Values: 30/sec, 20/sec, 10/sec, 8/sec, 6/sec, 5/sec, 4/sec, 3/sec, 2/sec

Sets the rate at which a keyboard key will automatically repeat when held down, expressed in characters per second. Some operating systems, such as DOS, honor this initial setting and use it for run-time operations. Other operating systems, such as Windows, assume complete control of the Typematic Rate, and do not honor this setting.

Typematic Delay

Values: 250ms, 500ms, 750ms, 1 sec

Sets the amount of time a keyboard key must be held down before it begins automatically repeating. Some operating systems, such as DOS, honor this initial setting and use it for run-time operations. Other operating systems, such as Windows, assume complete control of the Typematic Delay, and do not honor this setting.

BACK TO MISC

Board Menu

The Board menu configures PCI interrupts, enables and disables ISA interrupts, and configures hardware monitoring interrupts.

```
+ ------------------------- ---------------------------- + ------------------
- +
| Misc Control                                          |Daniels board
|
| ------------------------- ---------------------------- |presence override.
|
| Daniels Override              [Disabled]              |
|
| FPGA base I/O address         [0xCA0]                 |
|
| ISA Bus                       [Enabled]               |
|
| 82574 Ethernet                [Enabled]               |
|
|                                                       |
|
| PCI Interrupt Configuration                           |
|
| ------------------------- ---------------------------- |
|
| PCI INT A routing             [IRQ 11]                |
|
```

```
| PCI INT B routing             [IRQ 11]                  |
|
| PCI INT C routing             [IRQ 11]                  |
|
| PCI INT D routing             [IRQ 9]                   |
|
| PCI INT E routing             [IRQ 9]                   |
|
| PCI INT F routing             [IRQ 9]                   |
|
| PCI INT G routing             [IRQ 9]                   |
|
| PCI INT H routing             [IRQ 9]                   |
|
|                                                         |
|
|                                                         |
|
+ -------------------------- ---------------------------- + ------------------
- +
```

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Daniels Override

Values: Enabled, Disabled

This parameter should always set to disabled.

FPGA base I/O address

Values: 0xCA0, 0xC90

Sets the base I/O address (16 bytes) for the FPGA control registers.

ISA Bus

Values: Enabled, Disabled

Enables or disables subtractive I/O and memory decodes on the ISA (PC/104) bus.

82574 Ethernet

Values: Enabled

Enables or disables the 82574 Ethernet controller.

PCI Interrupt Configuration

Values: Auto, IRQ 5, IRQ 9, IRQ 10, IRQ 11

Sets PCI interrupts. All four PCI interrupts can be shared without conflict, but in certain high performance hardware configurations, the assignment of separate IRQs can reduce IRQ latency. Make sure there are no conflicts with the ISA IRQ settings.

BACK TO BOARD

Video Menu

The Video menu configures display device settings.

```
+ ------------------------ ---------------------------- + ------------------
- +
|                                                       |Select video boot
|
| Display Device Configuration                          |display.
|
| ------------------------ ---------------------------- |Some modes may
|
| Video Boot Display            [CRT]                   |require a different
|
| LCD Flat Panel Type           [1024x768]              |Video BIOS support.
|
| Panel Fitting                 [Default]               |
|
| Video Frame Buffer Size       [32MB]                  |
|
|                                                       |
|
+ ------------------------ ---------------------------- + ------------------
- +
```

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Video Boot Device

Values: CRT, LFP, CRT+LFP

Selects the video boot device.

LCD Flat Panel Type

Values: Default, 640x480, 800x600, 1024x768 1280x1024, 1400x1050 Reduced Blanking, 1400x1050 non-Reduced Blanking, 1600x1200, 1280x768, 1600x1050, 1920x1200

Selects the flat panel type.

Panel Fitting

Values: Default, Center All, Stretch All, Stretch Text, Stretch Graphics

Selects the display expansion/centering setting.

Video Frame Buffer Size

Values: 32MB, 64MB, none

Selects the size of the frame buffer for on-board video.

BACK TO VIDEO

Chipset Menu

The Chipset menu configures chipset settings.

```
+ ------------------------- ---------------------------- + ------------------
- +
| UHCI #6 Remapping             [Enabled]                |Remap UHCI
controller|
|                                                        |#6 from Dev1A:Func2
|
| North Bridge Configuration                             |to Dev1D:Func3.
|
| ------------------------- ---------------------------- |
|
| Memory Bandwidth Throttling   [Enabled]                |
|
|   TM Lock                     [Disabled]               |
|
|   TS on DIMM                  [Enabled]                |
|
|   TS on Board                 [Disabled]               |
|
|                                                        |
|
+ ------------------------- ---------------------------- + ------------------
- +
```

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UHCI #6 Remapping

Values: Enabled, Disabled

Enables or disables UHCI #6 remapping from Dev1A:Func2 to Dev1D:Func3.

Memory Bandwidth Throttling

Values: Enabled, Disabled

Enables or disables memory bandwidth throttling.

TM Lock

Values: Enabled, Disabled

Enables or disables thermal management register lock.

TS on DIMM

Values: Enabled, Disabled

Enables or disables bandwidth throttling using the thermal sensor on the DIMM.

TS on Board

Values: Enabled, Disabled

Enables or disables bandwidth throttling using the thermal sensor on the board.

BACK TO CHIPSET

AdvancedCPU

The AdvancedCPU menu displays temperature and other CPU information.

```
+ -------------------------- ---------------------------- + ------------------
- +
|                                                        |Enable
|
| CPU Information
|Geyserville/Speedste-|
| -------------------------- ---------------------------- |
|
| CPU Model and Stepping:       1658                     |
|
| CPU Microcode Version:        2567                     |
|
| On-Die Thermal Sensor, *C to Overheat:        74       |
|
|                                                        |
|
| CPU Configuration                                      |
|
| -------------------------- ---------------------------- |
|
| Board is standard temperature                          |
|
| P7 Geyserville/Speedstep      [Enabled]                |
|
| SpeedStep Manual Speed (ET)   [1200 MHz]               |
|
| SpeedStep Lock                [Enabled]                |
|
| Dynamic FSB                   [Enabled]                |
|
```

Intel VT	[Disabled]
Microcode Update	[Enabled]
C1E	[Disabled]
C2E	[Enabled]
C4E	[Enabled]
Core Multi-Processing	[Enabled]

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P7 Geyserville/Speedstep

Values: Enabled, Disabled

Enabling this feature sets Geyserville/Speedstep processors to full speed.

SpeedStep Manual Speed

Values: 600, 1200

Selects a fixed CPU core frequency.

SpeedStep Lock

Values: Enabled, Disabled

When enabled, this option locks down the CPU speed. When disabled, load-based dynamic switching occurs.

Dynamic FSB

Values: Enabled, Disabled

Enables or disables processor dynamic FSB frequency switching. When enabled, this option allows virtual reduction of internal processing clock by one half. This option must be enabled if SpeedStep Manual Speed is set to 800 MHz.

Intel VT

Values: Enabled, Disabled

Enables or disables Intel Virtualization Technology.

Microcode Update

Values: Enabled, Disabled

Enables or disables processor microcode update.

C1E
C2E
C4E

Values: Enabled, Disabled

Enables or disabled C1, C2, or C4 states. If the state is not supported, the option is always set to disabled.

Core Multi-Processing

Values: Enabled, Disabled

When disabled, the second execution core will not be visible to software and cannot be started via an SIPI message.

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